HUAN-LIN CHANG

Berkeley, CA 94703 | huanlin@berkeley.edu | +1 510 984 8666

Profile

A highly skilled engineer with 6+ years in the industry and academia with expertise in device modeling and circuit simulation. An out-of-the-box thinker with exceptional problem-solving skills and a relentless passion to explore new possibilities.

- ✓ SPICE Modeling
- ✓ Corner and Statistical Model
- ✓ Process Design Kit
- ✓ Hspice, Spectre, Eldo
- ✓ Model Quality Assurance
- ✓ Device-to-Circuit Interaction
- ✓ Verilog-A, C, Python, PERL
- ✓ FinFET IC Design Flow
- ✓ Post Layout Extraction

Professional Experience

UNIVERSITY OF CALIFORNIA | BERKELEY, CA Sep 2015 – Sep 2018 (expected)

Postdoctoral Researcher in BSIM group led by Professor Chenming Hu

- Interact with the industry consortium Compact Model Coalition (CMC) to debug and ensure the robustness of BSIM models. Represent BSIM group in CMC quarterly meetings since 2015.
- Provide solutions to model issues from foundries and IC design companies with the help of the EDA vendors.
- Develop quality assurance (QA) flows to enhance the quality of BSIM models.
- Manage code repositories on GitHub to eliminate unwanted bugs and speed up model development.
- Maintain BSIM website for archives and new releases of BSIM models to the public since 2016.
- Make technical manual of BSIM-CMG available online for easy access of the model users.
- Spearhead development of an ADMS (a Verilog-A to C translator)-compatible version of BSIM-CMG model with Ngspice circuit simulator to create a truly "license-free" environment for BSIM model usage.

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY (TSMC) | HSINCHU, TAIWAN

Principal Engineer in Technology Modeling Division Nov 2011 – Aug 2015

- Participated in 15+ SPICE model projects in collaboration with device, integration, TCAD, and PDK engineers in advanced technology nodes from 20-nm planar to 16-nm, 10-nm, 7-nm FinFETs.
- Measured silicon data of IV, CV, noise and extracted model parameters for SPICE models of core/IO, multi-Vt transistors and passive devices. Wrote PERL scripts to automate parameter extraction process for SPICE projects.
- Built digital (TT/SS/FF/SF/FS) and analog (SSA/FFA) corner models for IC design signoff.
- Built statistical models using principal component analysis (PCA) to enable Monte-Carlo analysis of the circuits.
- Studied device-to-circuit performance relations to suggest methods for design iteration reduction.
- Oversaw a team in building a modeling platform for flicker and thermal noise, resulting in a reduced 2-to-1-week project cycle time.
- Tested model quality in Verilog-A and simulator implementation (HSPICE, Spectre, Eldo) of new versions of SPICE model standards in collaboration with model developers and EDA vendors.
- Maintained and created TSMC Modeling Interface (TMI) modules in C for advanced model features like various layout effects, self-heating effects, and flicker noise corners.

Affiliations

IEEE Member | 2007 – 2018
IEEE Member of Electron Devices Society | 2007 – 2018
IEEE Member of Solid-State Circuits Society | 2007 – 2018

Education

NATIONAL TAIWAN UNIVERSITY | TAIPEI, TAIWAN Jun 2011

Doctor of Philosophy (Ph.D.) in Electronics Engineering

- Thesis Title: Physical Mechanisms and SPICE Modeling of Resistive Random Access Memory
  Advisor: Professor Chee Wee Liu

NATIONAL TAIWAN UNIVERSITY | TAIPEI, TAIWAN Jun 2006

Bachelor of Science (B.S.) in Electrical Engineering

Skills

Programming: Verilog-A | C/C++ | Python | PERL | Matlab | Linux Shell Scripts
Circuit simulators: HSPICE | Spectre | Eldo | ADS | Ngspice
Layout editor: Virtuoso
Others: Git | GitHub | Gitbook

Languages

English: Fluent
Mandarin: Native speaker

Selected Publications

JOURNAL PAPERS

- H. Agarwal, P. Kushwaha, J. P. Duarte, Y.-K. Lin, A. Sachid, **H.-L. Chang**, S. Salahuddin, and C. Hu, "Designing 0.5V 5nm HP and 0.23V 5nm LP NC-FinFETs with improved Ioff sensitivity in presence of parasitic capacitance," IEEE Trans. on Electron Devices, vol. 65, no. 3, pp. 1211-1216, Mar. 2018.
- Y.-K. Lin, P. Kushwaha, J. P. Duarte, **H.-L. Chang**, H. Agarwal, S. Khandelwal, A. B. Sachid, M. Harter, J. Watts, Y. S. Chauhan, S. Salahuddin, and C. Hu, "New mobility model for accurate modeling of transconductance in FDSOI MOSFETs," IEEE Trans. on Electron Devices, vol. 65, no. 2, pp. 463-469, Feb. 2018.
- Y.-K. Lin, P. Kushwaha, H. Agarwal, **H.-L. Chang**, J. P. Duarte, A. B. Sachid, S. Khandelwal, S. Salahuddin, and C. Hu, "Modeling of back-gate effects on gate-induced drain leakage and gate currents in UTB SOI MOSFETs," IEEE Trans. on Electron Devices, vol. 64, no. 10, pp. 3986-3990, Oct. 2017.
- Y.-K. Lin, J. P. Duarte, P. Kushwaha, H. Agarwal, **H.-L. Chang**, A. Sachid, S. Salahuddin, and C. Hu, "Compact modeling source-to-drain tunneling in sub-10-nm GAA FinFET with industry standard model," IEEE Trans. on Electron Devices, vol. 64, no. 9 pp. 3576-3581, Sep. 2017.
- Y.-K. Lin, S. Khandelwal, J. P. Duarte, **H.-L. Chang**, S. Salahuddin, and C. Hu, "A predictive tunnel FET compact model with atomistic simulation validation," IEEE Trans. on Electron Devices, vol. 64, no. 2, pp. 599-605, Feb. 2017.
- Y.-K. Lin, S. Khandelwal, A. S. Medury, H. Agarwal, **H.-L. Chang**, Y. S. Chauhan, and C. Hu, "Modeling of subsurface leakage current in low V_{TH} short channel MOSFET at accumulation bias," IEEE Trans. on Electron Devices, vol. 63, no. 5, pp. 1840-1845, May 2016.
- C.-F. Huang, C.-Y. Peng, Y.-J. Yang, H.-C. Sun, H.-C. Chang, P.-S. Kuo, **H.-L. Chang**, C.-Z. Liu, and C. W. Liu, "Stress-induced hump effects of p-channel polycrystalline silicon thin-film transistors," IEEE Electron Device Lett., vol. 29, no. 12, pp. 1332-1335, Dec. 2008.
- **H.-L. Chang**, P.-S. Kuo, W.-C. Hua, C.-P. Lin, C.-Y. Lin, and C. W. Liu, "Reduction of crosstalk between dual power amplifiers using laser treatment," IEEE Microw. Wireless Compon. Lett., vol. 18, no. 9, pp. 602-604, Sep. 2008.
- W.-C. Hua, **H.-L. Chang**, T. Wang, C.-Y. Lin, C.-P. Lin, S. S. Lu, C. C. Meng, and C. W. Liu, "Performance enhancement of the nMOSFET low noise amplifier by package strain," IEEE Trans. Electron Devices, vol. 54, no.

1, pp. 160-162, Jan. 2007.

CONFERENCE PAPERS

- J. P. Duarte, S. Khandelwal, A. I. Khan, A. Sachid, Y.-K. Lin, **H.-L. Chang**, S. Salahuddin, and C. Hu, "Compact models of negative-capacitance FinFETs: Lumped and distributed charge models," in Proc. IEEE International Electron Devices Meeting (IEDM), 30.5.1-30.5.4, Dec. 2016.
- P. Kushwaha, H. Agarwal, Y. S. Chauhan, M. Bhoir, N. R. Mohapatra, S. Khandelwal, J. P. Duarte, Y.-K. Lin, **H.-L. Chang**, and C. Hu, "Predictive effective mobility model for FDSOI transistors using technology parameters," in Proc. International Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 448-451, Aug. 2016.
- H. Agarwal, P. Kushwaha, Y. S. Chauhan, S. Khandelwal, J. P. Duarte, Y.-K. Lin, **H.-L. Chang**, C. Hu, H. Wu, and P. D. Ye, "Modeling of GeOI and validation with Ge-CMOS inverter circuit using BSIM-IMG industry standard model," in Proc. International Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 444-447, Aug. 2016.
- P. Kushwaha, R. Agarwal, H. Agarwal, Y. S. Chauhan, S. Khandelwal, J. P. Duarte, Y.-K. Lin, **H.-L. Chang**, and C. Hu, "Modeling of threshold voltage for operating point using industry standard BSIM-IMG model," in Proc. International Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 216-219, Aug. 2016.
- **H.-L. Chang**, H.-C. Li, C. W. Liu, F. Chen, and M.-J. Tsai, "A parameterized SPICE macromodel of resistive random access memory and circuit demonstration," in Proc. Simulation of Semiconductor Processes and Devices (SISPAD), pp. 163-166, Sep. 2011.
- **H.-L. Chang**, H.-C. Li, C. W. Liu, F. Chen, and M.-J. Tsai, "Physical mechanism of HfO2-based bipolar resistive random access memory," in Proc. International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), pp. 110-111, Apr. 2011.
- **H.-L. Chang**, H.-C. Chang, S.-C. Yang, H.-C. Tsai, H.-C. Li, and C. W. Liu, "Improved SPICE macromodel of phase change random access memory," in Proc. International Symposium on VLSI Design, Automation and Test (VLSI-DAT), pp. 134-137, Apr. 2009.
- **H.-L. Chang**, P.-T. Lin, W.-C. Hua, C.-P. Lin, C.-Y. Lin, C. W. Liu, T.-Y. Yang, and G.-K. Ma, "Differential power combining technique for general power amplifiers using lumped component network," in Proc. Asia-Pacific Microwave Conf. (APMC), pp. 500-503, Dec. 2006.
- W.-C. Hua, P.-T. Lin, C.-P. Lin, C.-Y. Lin, **H.-L. Chang**, C. W. Liu, T.-Y. Yang, and G.-K. Ma, "Coupling effects of dual SiGe power amplifiers for 802.11n MIMO applications," in Proc. Radio Frequency Integrated Circuits (RFIC) Symp., pp. 65- 68, Jun. 2006.