Stress-Induced Hump Effects of p-Channel Polycrystalline Silicon Thin-Film Transistors

Ching-Fang Huang, *Student Member, IEEE*, Cheng-Yi Peng, *Student Member, IEEE*, Ying-Jhe Yang, *Student Member, IEEE*, Hung-Chang Sun, Hung-Chih Chang, Ping-Sheng Kuo, *Student Member, IEEE*, Huan-Lin Chang, *Student Member, IEEE*, Chee-Zxaing Liu, and Chee Wee Liu, *Senior Member, IEEE*

***Abstract*—Positive bias temperature instability in p-channel polycrystalline silicon thin-film transistors is investigated. The stress-induced hump in the subthreshold region is observed and is attributed to the edge transistor along the channel width direction. The electric field at the corner is higher than that at the channel due to thinner gate insulator and larger electric flux density at the corner. The current of edge transistor is independent of the channel width. The electron trapping in the gate insulator via the Fowler–Nordheim tunneling yields the positive voltage shift. As compared to the channel transistor, more trapped electrons at the edge lead to more positive voltage shift and create the hump. The hump is less significant at high temperature due to the thermal excitation of trapped elections via the Frenkel–Poole emission.**

***Index Terms*—Hump, poly-Si, positive bias temperature instability (PBTI), thin-film transistor (TFT).**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted great interest in recent years for applications in active matrix liquid crystal displays. Negative bias temperature instability in p-channel MOSFETs [1] and TFTs [2] is a severe reliability problem. On the other hand, positive bias temperature instability (PBTI) in p-channel MOSFETs seems negligible [3]. Because PMOS poly-Si TFTs are rather stable and cost-effective than CMOS poly-Si TFTs [4], positive bias would apply to gate electrode when using only p-channel TFTs in the panel circuit design [5]. As a result, PBTI on p-channel TFTs would also become a reliability topic in the circuits in the displays.

II. Experiments

The LTPS TFTs were fabricated with top-gate structure. Buffer oxide layer was first deposited by plasma-enhanced chemical vapor deposition (PECVD) on the glass substrate. Next, a 40-nm-thick active layer of amorphous Si was deposited by PECVD on the buffer oxide and then crystallized by excimer laser annealing to form the poly-Si channel with a grain size of 0.3 μm [6]. Following that, a 120-nm physically thick $\mathrm{SiN}_x/\mathrm{SiO}_2$ gate oxide stack layer was deposited by PECVD. The equivalent oxide thickness (EOT) is 100 nm. After the source/drain formation, Mo was deposited as the gate metal.

Manuscript received September 8, 2008; revised September 29, 2008. This work was supported by the National Science Council, Taiwan, under Contracts NSC 97-2221-E-002-229-MY3 and 97-2221-E-002-232-MY3. The review of this letter was arranged by Editor J. K. O. Sin.

The authors are with the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 106, Taiwan (e-mail: chee@cc.ee.ntu.edu.tw).

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Digital Object Identifier 10.1109/LED.2008.2007306

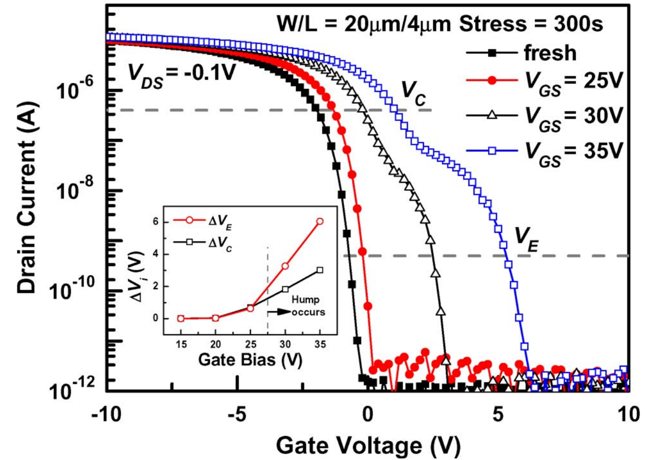

Fig. 1. Transfer characteristics of p-channel LTPS TFTs under different gate bias stress for 300 s. The hump is observed in the subthreshold region. The inset shows the voltage shift for the channel and edge transistors versus gate bias stress.

III. Results and Discussion

The transfer characteristics of p-channel LTPS TFTs under different gate stress voltages for 300 s are shown in Fig. 1. The devices are measured at $V_{\mathrm{DS}} = -0.1$ V. The channel width (W) and length (L) are 20 and 4 μm, respectively. The gate is stressed under a positive voltage, while the source and drain are grounded. Humps at the transfer curves are observed for devices after gate stress bias larger than 30 V. To simplify the analysis, two reference voltages V_C (channel transistor) and V_E (edge transistor) are defined at constant currents

$$V_C \equiv V_{\mathrm{GS}}@I_{\mathrm{DS}} = 10^{-7} \times \left(\frac{W}{L}\right) \quad (1)$$

$$V_E \equiv V_{\mathrm{GS}}@I_{\mathrm{DS}} = 5 \times 10^{-10} \quad (2)$$

$$\Delta V_i \equiv V_i(\mathrm{stress}) - V_i(\mathrm{fresh}), \qquad i = C, E. \quad (3)$$

From the inset of Fig. 1, ΔV_C and ΔV_E show the same stress-induced behavior for V_{GS} less than 25 V. However, the

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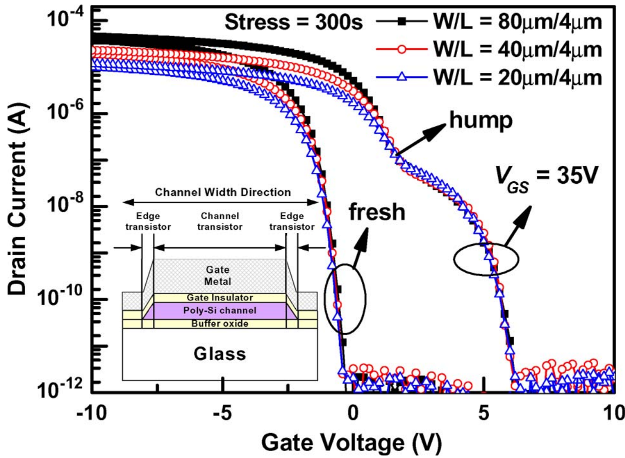

Fig. 2. Transfer characteristics of devices with different channel widths. The onset of the hump is observed at the same gate voltage and drain current. The inset shows the schematic structure of edge transistors along the channel width direction.

ΔV_E increases faster than ΔV_C when V_{GS} is larger than 25 V. The p-channel TFTs with the same channel length but different channel widths are compared under the gate stress voltage of 35 V for 300 s. Fig. 2 shows that all fresh devices with different widths have similar subthreshold behavior, and humps are observed after positive bias stress. Interestingly, the hump occurs at the same gate voltage and drain current for devices of different channel widths, suggesting that the hump is due to the edge transistor and independent of the channel width (inset of Fig. 2). Note that drain current decreases with channel width and is dominated by the channel transistor.

The cross-sectional scanning electron microscopy (SEM) image of the TFT along the channel width direction is shown in Fig. 3(a). The EOT on the wedge is $\sim$12% thinner than that on the channel. As a result, the average electric field at edge is $\sim$1.3$\times$ higher than that in the channel due to the combination of thinner EOT and larger electric flux density at the corner [7]. Fig. 3(b) shows the simulated electric field distribution at the channel and the corner for $V_{\mathrm{GS}} = 35$ V. The electric field is 3.4 MV/cm in the channel transistors, while it varies from 6.1 to 9.4 MV/cm along the corners (edges). The larger field at the edge transistor yields a larger Fowler–Nordheim (F-N) tunneling current from poly-Si to the gate electrode, and more electrons are trapped in the gate insulator of the edge transistor (inset of Fig. 5). As a result, the threshold voltage at the edge transistor shifts to a more positive voltage than the channel transistor, and the hump is formed. The humps previously reported in MOSFETs and poly-Si TFTs were observed for fresh devices without stress and can be overcome by optimizing the process [8], [9]. However, the reliability issue is even severer in this case since the hump is only observed after stress. As long as the active poly-Si layer is defined by isotropic wet etching process, the edge transistor always exists and may turn on after sufficient stress. The anisotropic etching and corner rounding can remove the edge transistors to some extent [10]. The ring-type channel can completely remove the edge transistors but is not practical to circuit applications [11].

The temperature dependence of hump characteristics is shown in Fig. 4. The devices are stressed at $V_{\mathrm{GS}} = 35$ V for 300 s. The hump is less significant at higher temperature, i.e., ΔV_E (high temperature) is smaller than ΔV_E (25 °C).

At higher temperature, the number of electrons trapped in gate insulator may increase due to higher electron thermal velocity in $\mathrm{SiO_2}(v_{\mathrm{th}})$ [12]. The electron capture time constant is inversely proportional to $\sigma_n v_{\mathrm{th}} n$ [13], [14]. The electron density (n) varies slightly ($\sim$0.1%) by numerical simulation and can be regarded as constant at different temperature for V_{GS} of 35 V. The electron capture cross section (σ_n) does not have strong temperature dependence, and the electron trapping as a function of temperature only relates to v_{th}, which is proportional to the square root of temperature. This statement is valid for Coulomb-attractive traps and neutral traps, which have larger σ_n. The Coulomb-repulsive traps can be temperature activated, but their cross section is relatively small [15]. Therefore, the capture rate of most active traps in our insulator has no Arrhenius dependence on temperature. Notice that the temperature dependence on F-N injection is negligible based on our quantum-mechanical simulation and the study in [16].

On the other hand, the trapped electrons can be reemitted by Frenkel–Poole (F-P)-type emission simultaneously under the stress. The F-P emission is thermally activated, and the barrier height for emission is electric field dependent (inset of Fig. 5). As shown in Fig. 4, the hump is less significant at higher temperature, suggesting that the detrapping by the F-P-type emission is the dominant process. In addition, the subthreshold slope (SS) is slightly degraded and may be attributed to the increase of density of interface traps (ΔD_{it}). The ΔD_{it} also contributes to ΔV_i, and the impact of trap generation should be considered. SS_C and SS_E are defined as the SS of channel and edge transistors, respectively. The fresh subthreshold current increases with increasing channel width (Fig. 2), indicating that the fresh subthreshold characteristics are dominated by channel transistor. In addition, the degraded SS_C and SS_E were obtained as fitting parameters to fit the measured I–V curve by using the superposition model of channel and edge transistors. However, the $\Delta\mathrm{SS}_E$ cannot be obtained directly since the edge transistor is invisible before stress and fresh SS_E is unknown. Because the average electric field for edge transistor is $\sim$1.3$\times$ larger than that of channel transistor, it is reasonable to assume $\Delta\mathrm{SS}_E$ to be $k\Delta\mathrm{SS}_C$, where k is ranging from 1 to 1.5, as shown in the error bar of edge transistor curve in Fig. 5. Consequently, the net trapping as a function of temperature $(\Delta V_{i,\,\mathrm{total}}(T))$ can be expressed as

$$\Delta V_{i,\,\mathrm{total}}(T) = \Delta V_{i,\,\mathrm{trapping}}(T) - \Delta V_{i,\,\mathrm{detrapping}}(T) + \Delta V_{i,\Delta D_{\mathrm{it}}}(T) \quad (4)$$

where $\Delta V_{i,\,\mathrm{total}}(T)$ is obtained from the experiment and $\Delta V_{i,\,\mathrm{trapping}}(T)$ is proportional to the square root of temperature. To obtain ΔV_i due to ΔD_{it}, assume that all the interfacial states below the charge neutral level are donor type and that ΔD_{it} is constant within ψ_B below the charge neutral level, where ψ_B is the potential difference between Fermi potential and intrinsic potential. The extracted $\Delta V_{i,\Delta\mathrm{Dit}}$ is $\sim$0.16 V for channel transistor at 25 °C. However, the calculated $\Delta V_{i,\Delta\mathrm{Dit}}$ is not accurate because the actual distribution of ΔD_{it} is not constant. In addition, the interfacial states can be either acceptor

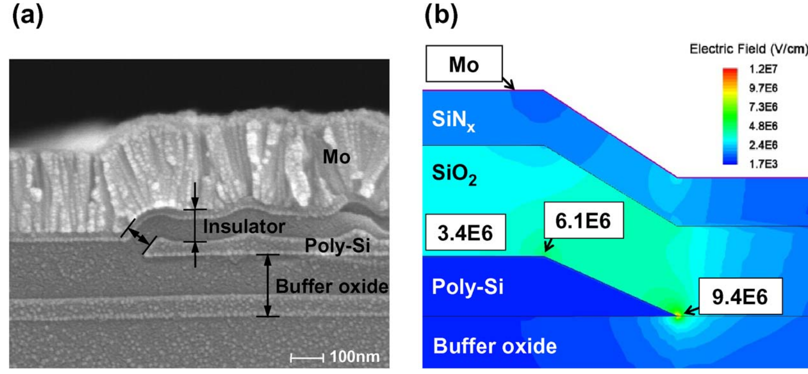

Fig. 3. (a) SEM image along the channel width direction. The EOT at the edge is ∼12% thinner than that at the center. (b) The simulated electric field distribution at the channel and the corner for $V_{\mathrm{GS}} = 35$ V. The electric field at the corner is larger than that at the channel.

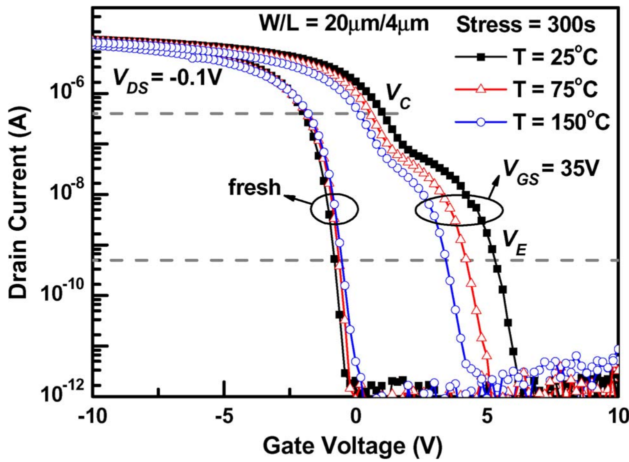

Fig. 4. Temperature dependence of hump characteristics. The hump is less significant at higher temperature due to electron detrapping by F-P emission.

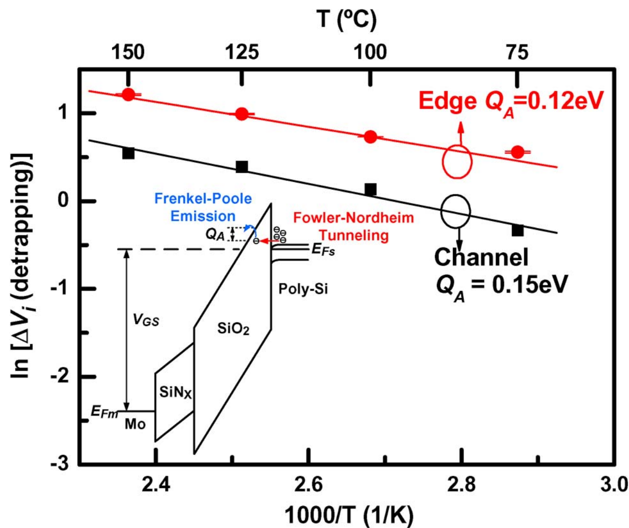

Fig. 5. Arrhenius plot of the electron detrapping process. The higher electric field at the corner results in smaller activation energy. The inset shows the charge trapping (F-N tunneling) and detrapping (F-P emission) mechanisms.

type or donor type since the charge neutral level may not coincide with midgap level. As a result, this may lead to some uncertainty in the evaluation of $\Delta V_{i,\Delta\mathrm{Dit}}$.

Based on above discussions, $\Delta V_{i,\,\mathrm{detrapping}}(T)$ is used to characterize the number of emitted electrons in the gate insulator at elevated temperatures. Furthermore, we have to assume no significant F-P-type emission (detrapping) at room temperature as a basis for the activation energy calculation. Fig. 5 shows the Arrhenius plot of the charge detrapping process. The number of emitted electrons is determined by F-P-type emission

$$\Delta V_{i,\,\mathrm{detrapping}}(T) \sim E \exp\left[\frac{q\left(\phi_B - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right] \equiv E \exp\left[\frac{q(Q_A)}{kT}\right] \quad (5)$$

where E, ε_i, and ϕ_B are the electric field, gate insulator permittivity, and trap level depth, respectively. Q_A is the activation energy of the F-P process, as shown in the inset of Fig. 5. From the Arrhenius plot, the extracted activation energies are 0.12 eV for edge transistor and 0.15 eV for channel transistor. As the electric field increases, the energy barrier height (Q_A) for electron detrapping is lowered. Consequently, higher electric field at the corner results in smaller Q_A of the edge transistor. On the other hand, the trap level (ϕ_B) is only related to the properties of the insulator and is extracted to be ∼0.9 eV for both channel and edge transistors [17].

IV. Conclusion

The PBTI in poly-Si TFTs is comprehensively studied. The stress-induced hump results from more trapped electrons in the insulator at the corner due to higher electric field. The hump is less significant at higher temperature due to F-P emission.

Acknowledgment

The authors would like to thank the Toppoly Optoelectronics Corporation, Taiwan, for the chip fabrication.

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