Modeling of Advanced RF Bulk FinFETs

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***Abstract*— The modeling of the advanced RF bulk FinFETs is presented in this letter. Extensive S-parameter measurements, performed on the advanced RF bulk FinFETs, show 31% improvement in cutoff frequency over recent work [1]. The transistor's characteristics are dominated by substrate parasitics at intermediate frequencies (0.1–10 GHz) and gate parasitics at high frequencies (above 10 GHz). The Berkeley short-channel IGFET model-common multi gate model is improved to account for the impact of substrate coupling on the RF parameters. The model demonstrates excellent agreement with the measured data over a broad range of frequencies. The model passes AC, DC and RF symmetry tests, demonstrating its readiness for (RF) circuit design using FinFETs.**

***Index Terms*— RF FinFET, compact model, cut-off frequency, Berkeley short-channel IGFET model-common multi gate (BSIM-CMG).**

I. Introduction

THE system on chip (SoC) integrates complex, high power devices with high frequency (HF) transceiver blocks, resulting in better power consumption and RF integration [2]. According to the 2016 prediction of the ITRS 2.0 roadmap [3], FinFET will continue the scaling trend of CMOS transistors to the 5nm technology node and beyond. In the light of RF FinFET having great potential for high-frequency wireless communication market, a complete compact model of the RF FinFET is the need of the hour. This work addresses this need. The Berkeley short-channel IGFET model-common multi gate (BSIM-CMG) is the first industry standard compact model for the FinFET [4]. However, at high frequencies, the parasitic resistances and capacitances greatly influence the FinFET's characteristics. Hence, the DC compact model alone is not sufficient to accurately predict the device behavior over a wide frequency range [5].

In this work, we report RF characteristics of the advanced bulk FinFET device supplied by the industry. The device shows an improvement of 31% in cutoff frequency as compared to previously reported value in [1]. The device behavior is modeled using BSIM-CMG model, which is improved in this work to account for the substrate effect [6]. Further, we propose a step-by-step DC and RF parameter extraction methodology, to show the importance of each RF submodule i.e., thermal, substrate and gate network modules. The data reported in this work is measured on a ground-signal-ground (G-S-G) pad set in an industrial lab. Short-open-load-through (SOLT) method is used for calibration and the parasitic elements from pad to device are de-embedded using open-short structures. The letter is organized as follows: in section II, we discuss RF FinFET modeling strategy, its validation, and parameter extraction procedure. Conclusions are presented in section III.

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II. RF FinFET Modeling and Validation

The first step towards accurate RF modeling is the extraction of DC parameters from state-of-the-art experimental data. The DC parameter extraction procedure starts with the gate capacitance vs. gate voltage plot as shown in Figure 1(a). Different process parameters such as oxide thickness, flatband voltage, and parameters for quantum mechanical confinement effects are extracted in this step. Then, parameters related to real device effects like mobility degradation, series resistance, and drain induced barrier lowering (DIBL) are extracted from current (I_{ds}) and transconductance (g_m) vs. gate voltage (V_{gs}) characteristics. Next step is to extract the parameters related to velocity saturation, channel length modulation, and thermal resistance from I_{ds} and output conductance (g_{ds}) vs. drain voltage (V_{ds}) characteristics. The complete list of parameters can be found in [4]. Figure 1(b) and Figure 1(c) show the model results using above mentioned procedure. Apart from modeling the current, accurate modeling of derivatives is also crucial, as they set the low-frequency values of small signal parameters discussed in the next section.

A. Thermal Network Extraction

Figure 2(a) shows real Y_{22} vs. frequency characteristics. In the absence of self-heating effect (SHE), the low frequency value of Real Y_{22} will match the DC value (i.e., g_{ds} extracted from Figure 1(c)). However, short channel devices can experience severe self-heating effects, that depend on device geometry and operating bias conditions. The SHE also strongly depends on the frequency of operation and is more significant at DC and low frequencies. As a result, the Real Y_{22} value at higher frquencies differs from its DC value and this characteristic is used to extract the thermal capacitance (C_{th}). However, this difference is very small in bulk FinFETs, as channel heat dissipates easily in bulk FinFETs [9] compared to FDSOI [10]–[14] or SOI FinFETs [15], [16]. Note that the thermal resistance (R_{th}) and series resistance values are

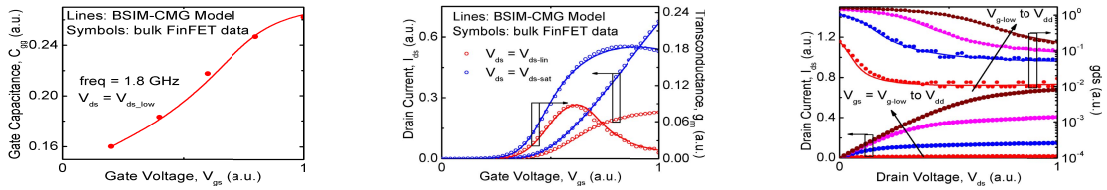


Fig. 1. Model results (a) C_{gg} vs. gate voltage, where C_{gg} is extracted from imaginary part of $Y_{11}/(2\pi \cdot f)$. (b) The drain current and transconductance vs. gate voltage characteristics. Bias conditions are: $V_{ds} = V_{dslin}$ and V_{dssat}. (c) The drain current and output conductance vs. drain voltage characteristics. $V_{gs} = V_{g-low}$ to V_{dd}. Here V_{dd} denotes the power supply. The device under test is supplied by the industry, and therefore limited device details are reported here. The device has number of fingers (NF) = 64 and number of fins (Nfin) = 4. Symbols: Experimental Data, Lines: BSIM-CMG model.

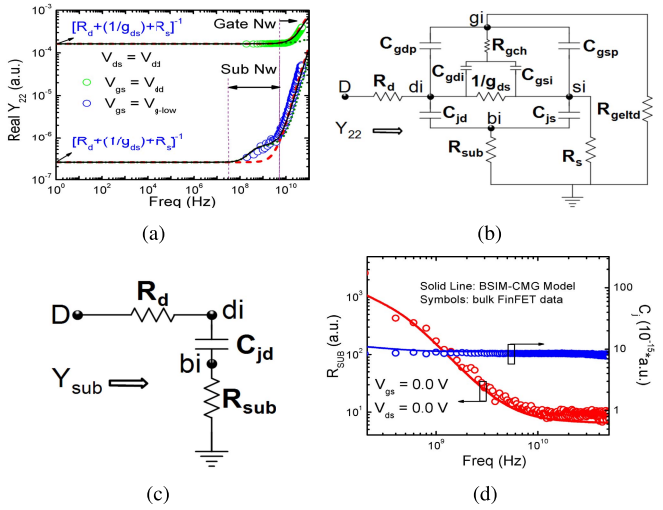


Fig. 2. (a) Measured real part of Y_{22} for two values of gate voltage at $V_{ds} = V_{dd}$. In the presence of the gate and the substrate network, the real part of Y_{22} will asymptotically reach a value equal to $\frac{1}{R_d+(R_{sub}||R_s||R_{geltd})}$ (not shown here). (b) Simplified two-port network is illustrated for the calculation of Y_{22} parameter. D denotes drain node. gi (gate), di (drain), si (source) and bi (body) represent internal nodes. (c) Simple equivalent circuit of the substrate components for the device in the off-state [7], [8]. 1-resistor network is used to capture the impact of substrate [6]. (d) Measured and extracted R_{sub} and junction capacitance at $V_{gs} = V_{ds} = 0V$. Dashed line: The model without substrate network (old model). Dotted line: The model without gate network. Symbols: Experimental Data, Solid Lines: BSIM-CMG model (improved model).

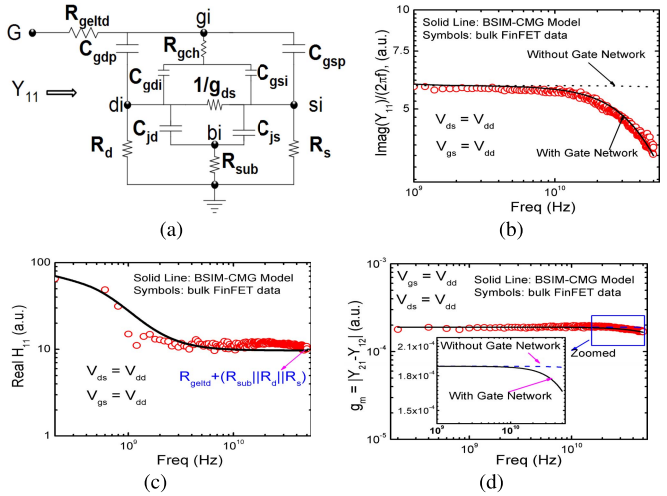


Fig. 3. (a) Simplified two-port network is illustrated for the calculation of Y_{11} parameter. G denotes gate node. (b) Measured imaginary part of $Y_{11}/(2\pi f)$. (c) Measured real part of H_{11} (gate resistance) vs. frequency characteristic. (d) Trans-conductance vs. frequency characteristics. Symbols: Experimental Data, Lines: BSIM-CMG model.

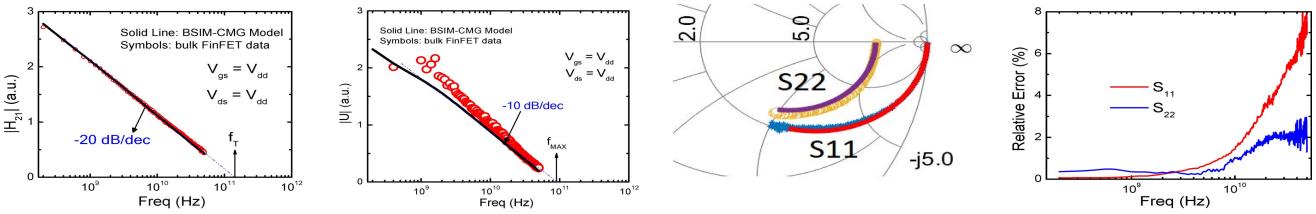
already extracted from Figure 1(b) and Figure 1(c). However, these parameters may be fine-tuned during RF parameter extraction to achieve a good fit.

B. Substrate Network Extraction

Figure 2(b) shows the simplified two-port network for the calculation of Y_{22}. This network can be understood more easily by calculating the individual RC time constants, associated with each of the thermal, substrate, and gate networks. At the intermediate frequency range (0.1-10GHz), the junction impedance reduces and becomes small enough, so that the RF signal at the drain couples to the bulk contact via the junction capacitance and substrate resistance [17], thereby influencing the Y_{22} vs. frequency characteristics. Figure 2(a) shows real Y_{22} for two (low and high) gate voltages. In the intermediate frequency range, real Y_{22} shows a transition at low gate voltage. This transition also exists at high gate voltage, but, it is not as prominent because the value of g_{ds} itself is high at large V_{gs}. The reason behind this transition is larger time constant of the substrate network, compared to gate network, because the junction capacitances (C_{js}, C_{jd}) of the bulk FinFET are nearly 2-3 orders of magnitude higher than the gate capacitance [17]. At low gate voltage (or in off-state), since the output conductance becomes very low, it further simplifies the circuit in Figure 2(b) to the simple equivalent circuit shown in Figure 2(c), in which the output network becomes a series connection of the junction capacitance and substrate resistance [17]. Hence, we have extracted the substrate network parasitic components in the off-state condition in the intermediate frequency range, as shown in Figure 2(d). Figure 2(a) to Figure 2(d) show that the real Y_{22} is dominated by the substrate network at low gate voltages in the off-state condition, whereas in the on-state, it is influenced by output conductance of the intrinsic device [18]. Hence, a proper extraction of DIBL, CLM, and the substrate network is required to capture the real Y_{22} accurately.

C. Gate Network Extraction

In the high frequency range (above 10GHz), real Y_{22} data show another transition, for both the gate voltages, which implies the involvement of another RC time constant coming from the gate network [19]. Thus, the gate parasitic components are extracted above 10GHz. Figure 3(a) shows the simplified two-port network for the calculation of Y_{11}. Total gate capacitance consists of intrinsic channel capacitance and device parasitic capacitances like fringing and overlap capacitances. Figure 3(b) shows imaginary Y_{11} vs. frequency characteristics, which are used to extract the gate capacitance C_{gg}. In addition to capacitances, the gate resistance is also a key



(a) (b) (c) (d)

Fig. 4. (a) Current gain $|H_{21}|$ variation with frequency. (b) Mason's unilateral power gain (U). (c) Smith chart validation for S_{11} and S_{22}. (d) Relative error vs. frequency characteristics for S_{11} and S_{22}. The model shows less than 10 % relative error at very high frequency range. This error can be reduced further using 5-R substrate network instead of 1-R substrate network at the cost of computation time [6]. Symbols: Experimental Data, Lines: BSIM-CMG model.

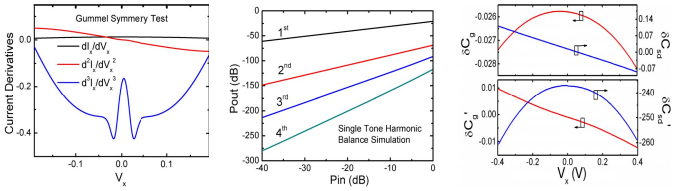
component of the gate network as both gate resistance (R_g) and gate capacitance (C_{gg}) together play an important role in determining the cutoff frequency f_t and maximum frequency of oscillation f_{max} of the transistor. Figure 3(a) shows that the gate resistance has two components: the distributed gate electrode resistance (R_{geltd}) and distributed channel resistance (i.e., virtual gate induced channel resistance R_{gch}) seen from the gate [20]. At low frequencies, both gate resistance components contribute to the input resistance (real H_{11}) [20], whereas at high frequencies, R_{gch} is bypassed by overlap and fringing capacitances, and the effective input resistance becomes $R_{geltd} + (R_{sub}||R_s||R_d)$ as shown in Figure 3(c). Figure 3(d) shows that the model is in good agreement with the extracted transconductance ($g_m = |Y_{21} - Y_{12}|$) data, which implies that the thermal, gate and substrate networks are extracted accurately.

D. RF Figure of Merit (FOM) Extraction

With the accurate parameter extractions of the thermal, substrate and gate networks as well as the junction capacitance, the model automatically shows good match with the current gain ($|H_{21}|$) as shown in Figure 4(a). The transit frequency (cutoff frequency) f_t is extracted by extrapolating the $|H_{21}|$ characteristic to 0 dB [21]. The transit frequency of the measured advanced bulk FinFET device is around 31% higher than the recently reported f_t value for a 14nm FinFET [1]. However, f_t only partially characterizes the ability of a device to operate at high frequencies. Another important FOM, that accounts for the gate resistance R_g and the drain-to-bulk capacitance C_{gd}, is the unilateral power gain U [21]. The unilateral power gain vs. frequency characteristic is shown in Figure 4(b) for the same bias point that was used to calculate $|H_{21}|$ and f_t. The value of the maximum frequency of oscillation f_{max} is extracted by extrapolating a line with a slope of -10 dB/decade from the U vs. frequency characteristic and then determining the frequency at which U becomes unity. The f_{max} of measured advanced RF bulk FinFET device is nearly equal to the recently reported f_{max} value for a 14nm FinFET [1]. Smith chart is shown in Figure 4(c) as the final validation of the model. The relative error between model and measurement data for S_{11} and S_{22} is shown in Figure 4(d). The model shows less than 10 % relative error at very high frequency range, implying that the input port components (gate network), output port components (substrate network) and the thermal effects have been optimized well.

E. RF Benchmark Test

For a compact model, it is important to properly model the symmetric nature of the device (i.e., symmetric source and drain terminals), because an asymmetric model may lead to inaccurate simulation results [22]. Therefore, we perform well-established tests for symmetries such as Gummel symmetry, AC symmetry, and Harmonic Balance. The Gummel symmetry test verifies the symmetry and continuity of the drain current and its higher order derivatives around $V_{ds} = 0V$ [23]. Figure 5(a) shows model results up to the 3^{rd} derivative. The symmetry and continuity of the derivatives help the model in passing the harmonic-balance (HB) test [24]. This test is important for evaluating the performance of RF circuits [22]. The model shows non-singular behavior for third and higher order harmonics at $V_{ds} = 0V$. The result of HB test is shown in Figure 5(b) which shows output power (P_{out}) vs. input power (P_{in}) characteristics for different harmonics. Model gives the correct slope of n for the n^{th} harmonic component [25]. In addition to the drain current, terminal charges and capacitances should also be symmetric (with respect to the source and drain terminals). This symmetry feature is tested using the AC symmetry test [26]. Figure 5(c) shows that the capacitance, transcapacitance and its higher order derivatives are symmetric and continuous around $V_{ds} = 0V$.



(a) (b) (c)

Fig. 5. (a) Gummel Symmetry Test results for the higher order derivatives of current at $V_{gs} = 0.8V$, (b) Analog/RF design quality assurance by Single-tone excitation Harmonic Balance test, (c) AC Symmetry Test results for the capacitance (δC_g), transcapacitance (δC_{sd}) and its higher order derivatives ($\delta C'_g$ and $\delta C'_{sd}$).

III. Conclusions

A detailed analysis of the frequency behavior of advanced RF bulk FinFETs has been performed. Modeling of substrate, gate and thermal effects is important for accurately capturing the high frequency behavior of the device. For the first time, a 1-resistor substrate network is implemented in the BSIM-CMG model to accurately capture all Y-parameters. A step-by-step DC and RF parameter extraction procedure is discussed across a wide range of frequencies. The model has successfully passed all symmetry tests and shows excellent match with the measured data, proving its readiness for high-frequency circuit design using FinFETs.

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