Modeling of GeOI and Validation with Ge-CMOS Inverter Circuit using BSIM-IMG Industry Standard Model

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***Abstract*—Recently, experimental Germanium CMOS devices and circuit are reported for advanced technology nodes for the first time. In this paper, we have modeled Germanium On Insulator (GeOI) device with industry standard compact model for independent double gate MOSFET (BSIM-IMG) with updated mobility model. It is shown that BSIM-IMG with updated mobility model accurately captures static characteristics for both n-channel and p-channel devices, and reproduces experimental CMOS inverter characteristics. This is the first time, when a compact model is validated on experimental CMOS circuit operation of GeOI.**

***Index Terms*—BSIM-IMG, Germanium on Insulator, Compact Model, Germanium CMOS.**

I. Introduction

Semiconductor industry has been driven by scaling of transistors for several decades. However, sub-micron scaling is limited by short channel effects, and there are efforts to improve drive current by enhancing mobility [1]. Germanium (Ge) is one of the important materials, which has regained attention owing to its high electron and hole mobility compared to silicon [2]. However, such efforts for high mobility materials are thwarted by the fabrication challenges as popular materials can support either n type (III-V compound semiconductor) or p type (Germanium) devices but not both, which are required for CMOS circuit designs [3]. There are, therefore, efforts for co-integration of hybrid channel devices for optimum CMOS performance (like Ge/strained silicon PMOS and compound semiconductor/silicon based NMOS) [4], [5]. Ge NMOS has poor drive current due to factors like high parasitic source drain resistance, high interface trap density etc. [6]–[8]. Recently, high performance Ge NMOS is reported in [9] and for the first time, experimental demonstration of Germanium on Insulator (GeOI) based CMOS circuits is carried in [10]. The next generation devices need a compact SPICE model to correctly design circuits before the real fabrication.

BSIM-IMG is a surface potential based compact model for independent double gate devices [11]. In BSIM-IMG model, surface potential at source and drain ends are first calculated by analytically solving surface potential equation using device related parameters, like effective oxide thickness at front

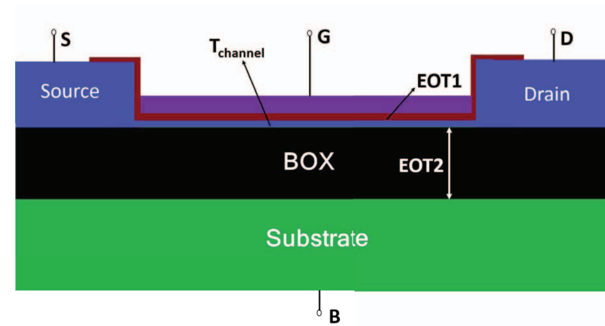

Fig. 1. Illustration of GeOI device under discussion. The devices considered has channel length L=40, 50, 70 and 90nm, EOT1=4.5nm, EOT2=400nm and two channel thickness of 15nm and 25nm. In this paper, we are modeling the GeOI devices with industry standard BSIM-IMG model, which is a surface potential based model. Channel width is 1μm for NMOS and 0.85 μm for PMOS, respectively.

(EOT1) and back (EOT2) side, channel thickness (T_{ch}) etc. [12]. This is followed by the calculation of inversion charge densities at source and drain ends, and finally terminal current and capacitances. Recently, effect of substrate depletion is added in the BSIM-IMG model [13] and initial guess for surface potential calculation is also updated [14]. The model has been through the rigorous testing by the BSIM group as well as by the industry experts under the aegis of the compact model coalition (CMC), and it has been declared as an industry standard model for independent double gate devices.

In this work, we have modeled GeOI devices with BSIM-IMG. Fig. 1 illustrate the simplified view of the GeOI device. To accurately model the GeOI characteristics, we have updated the mobility model of BSIM-IMG. The model is validated on experimental GeOI CMOS data including static characteristics of NMOS and PMOS, and voltage transfer characteristics (VTC) of CMOS inverter. This is the first time, when a compact model is validated on circuit operation for GeOI. This paper is organized as follows. Section II reports the updated mobility model for GeOI device. Validation results

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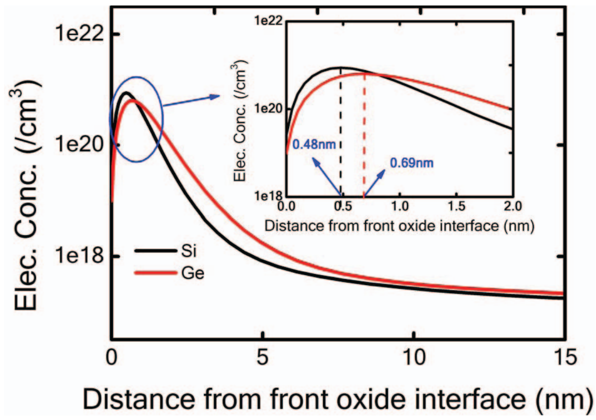


Fig. 2. Electron concentration as a function of distance from oxide-semiconductor interface in Si and Ge channel SOI MOSFET. Charge centroid for Ge is farther away from interface than that of silicon due to lower effective mass. This impacts the behavior of mobility with vertical electric field and enhances quantum mechanical effect on capacitance.

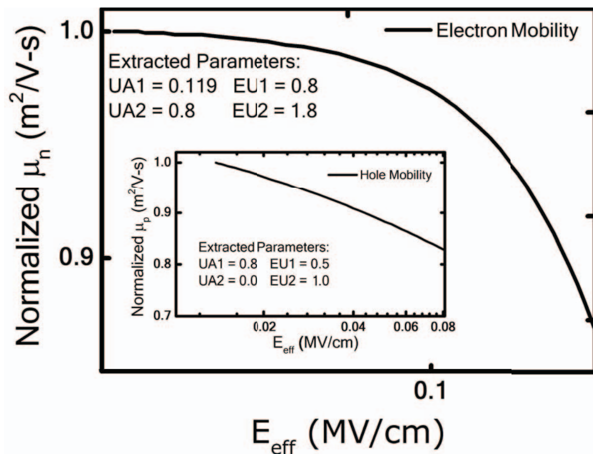
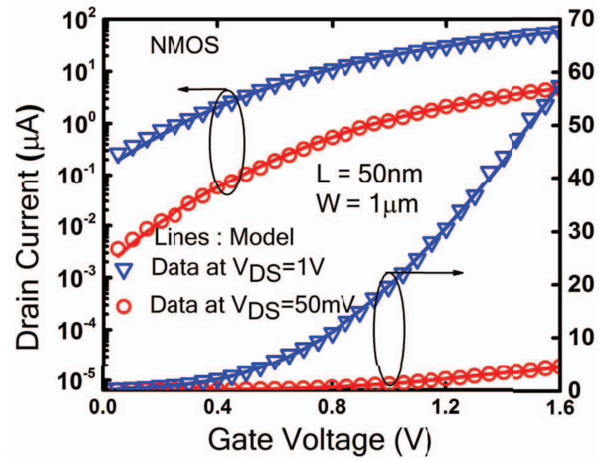
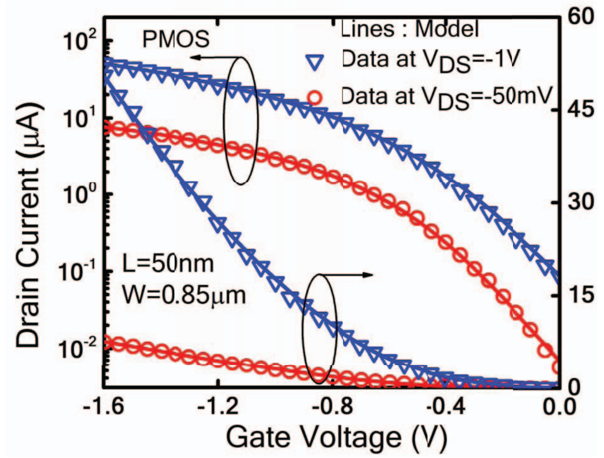


Fig. 3. Extracted electron mobility vs effective vertical electric field. Hole mobility is shown in the inset figure. During the extraction, we found that mobility degradation model accounting explicitly for both the phonon and SR scattering mechanisms (as in [15]) is needed and therefore the mobility model of the BSIM-IMG is updated similar to [16]. For PMOS, centroid is even farther than that in NMOS as effective mass of holes is less than effective mass of electrons, and therefore experiences reduced SR scattering.



(a)



(b)

Fig. 4. BSIM-IMG model validation with GeOI: (a) I_{DS}-V_{GS} characteristics of NMOS in linear and saturation region (b) I_{DS}-V_{GS} characteristics of PMOS in linear and saturation region. Low field mobility and source/drain resistance extracted from the model are 130 $cm^2/V-s$ and 150 Ω respectively for PMOS, and 135 $cm^2/V-s$ and 120 Ω respectively for NMOS.

are reported in Section III, and conclusion is drawn in Section IV.

II. Updated Mobility Model for GeOI

The effective mass of carriers in Ge is lower than that in silicon, and due to this the centroid of inversion layer in Ge is farther from the interface [17]. To illustrate this, inversion charge density along the increasing distance from the interface is compared for Si and Ge in Fig. 2. It is clearly observed that centroid in Ge is father from interface as compared to Si. This impacts the device electrical behavior as mobility has different dependence on vertical electric field, and gate capacitance reduces due to enhanced quantum mechanical effect (QME). First we will discuss the impact of centroid position on mobility, and gate capacitance is discussed later. During the parameter extraction process, we observed that the vertical field dependence of mobility in GeOI is different from silicon counterpart. This is due to the reason that inversion charge layer is away from the interface, and therefore surface roughness (SR) scattering is different in GeOI transistor. Currently, mobility degradation model of the BSIM-IMG model is same as that in other industry standard models [18] where the impact of vertical field on mobility is modeled by single exponent EU and coefficient UA. In this work, we have extended the mobility model proposed for p-channel Ge FinFet in [16] for both NMOS and PMOS GeOI to accurately model mobility degradation.

The new mobility model reads as

$$\mu_{eff} = \frac{\mu_0}{1 + UA1.E_{eff}^{EU1} + UA2.E_{eff}^{EU2} + UD.T1} \quad (1)$$

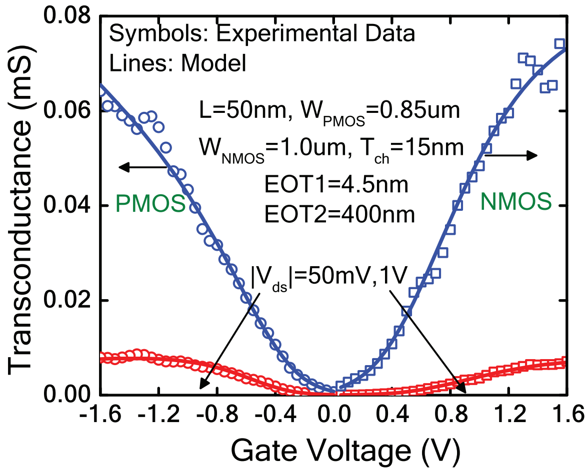


Fig. 5. Transconductance g_m vs gate voltage in linear and saturation region for NMOS and PMOS.

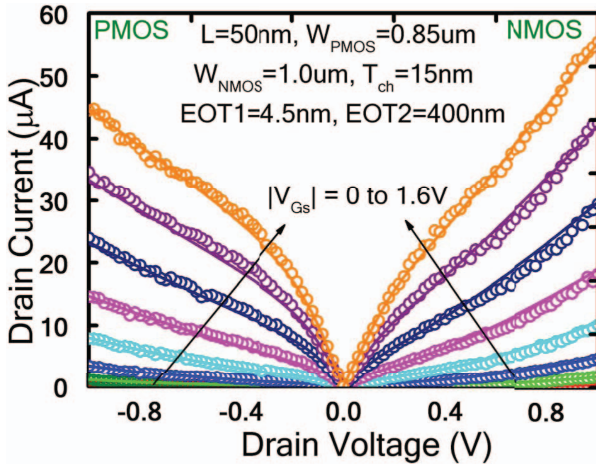


Fig. 6. $I_{DS} - V_{DS}$ characteristics of the NMOS and PMOS. Device dimensions: channel length L=50nm, channel thickness of 15nm, EOT1=4.5nm, EOT2=400nm. The model successfully captures the static characteristics including derivatives accurately for the bias ranges. Lines: Model, Symbols: Data

$$T1 = (1 + q_{ia}C_{ox})^{UCS} \tag{2}$$

where μ_0 is the low field mobility, E_{eff} is the effective vertical electric field, q_{ia} is the average inversion charge and C_{ox} is the oxide capacitance. $UA_{1/2}$, $EU_{1/2}$, UD, UCS are the model parameters. The variation of mobility with effective vertical electric field (E_{eff}) for holes and electrons as extracted from the model is shown in Fig. 3. For NMOS, the mobility has two slopes with E_{eff} corresponding to phonon and SR scattering mechanism [15] which is modeled by EU1 and EU2 along with the coefficients UA1 and UA2, respectively. For PMOS, even though here we could fit the characteristics with UA2=0, but in general it has been shown that such formalism is necessary for the PMOS as well [16].

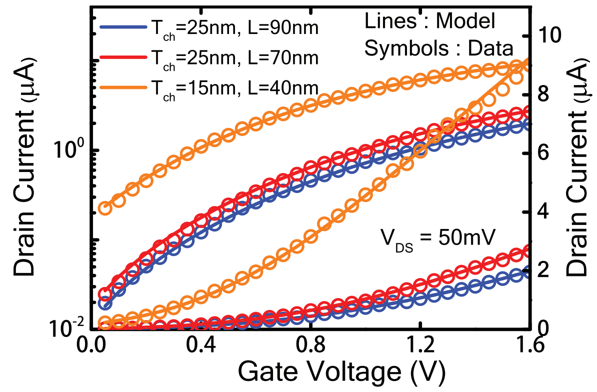


Fig. 7. Global fitting of multiple channel lengths with single modelcard for two different channel thickness : 25nm and 15nm.

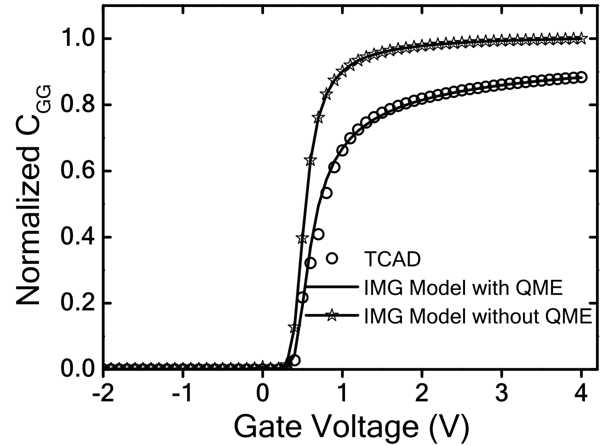
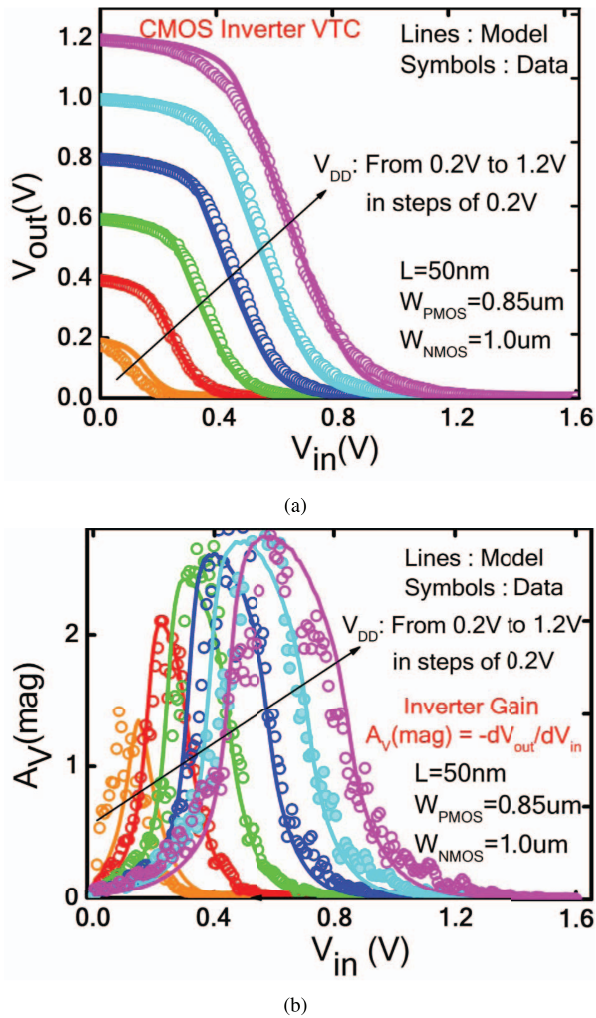


Fig. 8. Normalized gate capacitance vs front gate voltage. Charge centroid for Ge is away from that of silicon due to lower effective mass which reduced gate capacitance as the effective oxide thickness increases. In the BSIM-IMG model, this impact on capacitance is modeled through a correction term to the effective oxide thickness [19].

III. Results and Discussion

The BSIM-IMG model results with experimental data for NMOS is reported in Fig. 4(a) and for the PMOS in Fig. 4(b). Fig. 5 shows the transconductance g_m. The output characteristics $I_{DS} - V_{DS}$ at different gate voltages is shown in Fig. 6 (for both NMOS and PMOS). The parameter extraction procedure for BSIM-IMG is outlined in [19]. Low field mobility and source/drain resistance extracted from the model are 130 $cm^2/V - s$ and 150 Ω respectively for PMOS, and 135 $cm^2/V - s$ and 120 Ω respectively for NMOS. The BSIM-IMG model has continuous behavior across different regions of operation and captures the static characteristics including derivatives accurately for the bias ranges. The model is the physical and geometrically scalable which is further validated by excellent fitting of multiple channel length devices with global parameters as shown in Fig. 7 for two configurations of channel thickness: 25nm and 15nm.

We have seen in Fig. 2 that charge centroid in Ge is farther away from the surface. This increases the effective oxide



(a)

(b)

Fig. 9. BSIM-IMG model validation with GeOI CMOS inverter for V_{DD} ranging from 0.2V to 1.2V: (a) Voltage transfer characteristics (b) CMOS inverter gain vs input voltage. The BSIM-IMG accurately models the inverter behaviour, especially for V_{DD} up to 1V. It is important to note that the static characteristics are available up to $V_{DD} = 1V$, and the model is optimized till that bias range. Inverter gain is an important parameter as it determines noise margin, and is a function of derivatives which are accurately modeled.

thickness, and leads to gate capacitance reduction as shown in Fig. 8. In the BSIM-IMG model, this impact on capacitance is modeled through a correction term to the effective oxide thickness [19] which is observed in Fig. 8 to be fairly good in capturing the capacitance characteristics. Ge CMOS inverter VTC results are shown in Fig. 9(a) for different drain voltages while Fig. 9(b) shows the inverter gain vs input voltage characteristics. As can be observed from the figure, the BSIM-IMG model is able to accurately models the inverter behaviour. CMOS inverter gain is one of the important performance parameters as it defines the noise margin.

IV. Conclusion

In this paper, we have modeled experimental Germanium on Insulator devices using the BSIM-IMG model. BSIM-IMG with updated model of mobility degradation with vertical electric field can successfully capture the characteristics of GeOI devices. This is for the first time that a compact model capable of modeling not only static characteristics of the GeOI but also CMOS inverter.

V. Acknowledgement

Harshit Agarwal would like to thank Avirup Dasgupta, Chandan Yadav and Chetan Gupta of IIT Kanpur for technical discussions.
This work was supported in part by Semiconductor Research Corporation, in part by Science and Engineering Research Board (SERB) and in part by CSIR.

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