Modeling of Threshold Voltage for Operating Point using Industry standard BSIM-IMG Model

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***Abstract*—Threshold voltage is an important device parameter for MOSFET modeling as circuit designer needs to know the threshold voltage to bias the transistor in the required region of operation. In this paper, we have proposed an approach to calculate the threshold voltage for operating point information in the BSIM-IMG model which is the latest industry standard compact model for FDSOI transistors. The BSIM-IMG is the surface potential based model, and therefore threshold voltage is not explicitly available. The proposed model takes care of back-bias and other real device effects (CLM, DIBL etc) accurately. The model is developed to fulfill the demand of semiconductor companies for their commercial SPICE simulators and PDKs. We have shown model comparison with various popular threshold voltage extraction techniques. The model shows very good agreement with the measured data over wide range of device geometries, drain and body biases.**

I. Introduction

Recently Global Foundries has launched the industry's first 22 nm two-dimensional, fully-depleted silicon-on-insulator (FD-SOI) technology (22FDX technology platform) which provides the best path for cost-sensitive applications along with low-power, high-performance, and less-leakage facilities [1]. Presence of thinner gate oxide along with ultra-thin silicon body makes it a scalable structure even beyond 22 nm technology node [2]. The channel isolation from substrate through buried oxide (BOX) cuts off the substrate leakage current paths and reduced parasitic capacitances which makes FDSOI transistor very interesting device for analog and digital applications [3]. Due to the presence of ultra-thin BOX, FDSOI transistors has flexibility of tuning threshold voltage without varying channel doping, thus leading to excellent immunity from random dopant fluctuation and threshold voltage variability issues [4]. However thin BOX allows strong coupling from the drain through the lightly doped substrate and results in poor channel electrostatics [5]. Drawback of thin BOX has been eliminated by introducing the highly doped silicon layer (i.e., Back-plane, see Fig. 1) just below the BOX and has given facility of achieving different threshold voltage (V_{th}) flavors, i.e, low-V_{th} and high-V_{th} on single chip [6].

To capture the correct behavior of FDSOI transistors in complex circuit analyses, it is necessary to have a computationally efficient compact model which accounts for all real device effects. The BSIM-IMG model has surface potential based core hence all the electrical properties (i.e, charges,

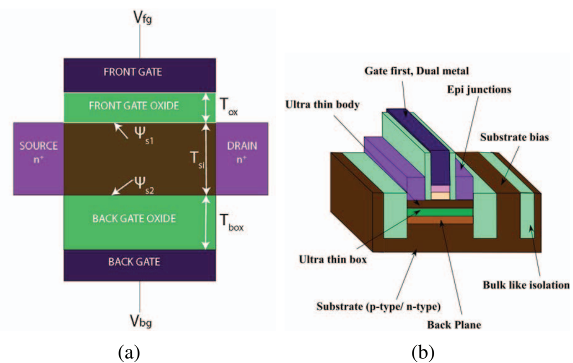

Fig. 1. (a) Basic framework for modeling independent double-gate MOSFETs. Device used in this work has front gate oxide thickness T_{ox} = 1.8 nm, back gate oxide thickness T_{box} = 10 nm, channel thickness T_{si} = 12 nm. Front and back gate voltages are V_{fg} and V_{bg}. Front and back gate surface potentials are ψ_{s1} and ψ_{s2}. (b) Schematic of a fully depleted silicon on insulator device (FDSOI). To have back-baising, the front side contact is used to the substrate/well. A shallow p++/n++ implant is performed below BOX to form a thin back-plane (BP) layer over a p-type substrate. Doping level difference between the BP and silicon body is used for a desired dynamic V_{th} shift [7].

current and capacitance) are calculated in terms of surface potential [8]–[10]. The model does not endorse threshold voltage based methodologies but from circuit designer point of view, it is important to know device's threshold voltage. Threshold voltage definition for FDSOI transistor has been reported in different ways. For highly doped channel, work [11] defines the threshold voltage as the gate voltage at which the minimum surface potential becomes $2\phi_b$, where ϕ_b is the Fermi potential. While for lightly doped channel, work [12] defines the threshold voltage as the gate voltage at which surface potential exceeds $\psi_s > 2\phi_b$. In this paper we have defined threshold voltage as the gate voltage at which drift current component becomes equal to diffusion current component and have proposed an analytical model of threshold volatge for the BSIM-IMG model which can be used for operating point information in commercial SPICE simulators. The paper is organized as follows: Analytical model for threshold voltage is derived in Section II. Results are discussed in Section III and finally, the conclusions are drawn in Section IV.

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II. Proposed Threshold Voltage Model

For a lightly-doped body, the inversion charge density is [13]:

$$Q_{in} = \sqrt{2N_c kT exp\left(\frac{q(\psi_{s1} - V_{ch})}{kT}\right) + (\epsilon_{si}E_{s2})^2} - \epsilon_{si}E_{s2} \quad (1)$$

where q is the electron charge, N_c is the conduction band density of states, k is the Boltzmann constant and T is the device temperature. ϵ_{si} and ϵ_{ox} are the permittivities of silicon and oxide. ψ_{s1} is front surface potential and V_{ch} is channel potential. E_{s2} is the back gate electric field and is expressed as (2) when back side is in weak inversion or depletion [13].

$$E_{s2} = \frac{\psi_{s1} - V_{bg}^*}{T_{si} + T_{box}\frac{\epsilon_{si}}{\epsilon_{ox}}} \quad (2)$$

where V_{bg}^* = V_{bg}-$\Delta\phi_2$, V_{bg} is back gate voltage and $\Delta\phi_2$ is back gate work function. $T_{\text{ox/box}}$ and $C_{\text{oxf/oxb}}$ are the front/back gate oxide thicknesses and capacitance respectively. $C_{\text{Si}} = \frac{\epsilon_{\text{Si}}}{T_{\text{Si}}}$ and T_{Si} is the silicon body thickness. After putting (2) in (1), inversion charge density can be expressed in terms of front surface potential equation as follows:

$$Q_{in}^2 + \frac{2Q_{in}\epsilon_{si}}{T_{si} + T_{box}\frac{\epsilon_{si}}{\epsilon_{ox}}}(\psi_{s1} - V_{bg}^*) - 2N_c kT\epsilon_{si}e^{\frac{\psi_{s1}}{Vt}} = 0 \quad (3)$$

where (3) is the implicit equation in inversion charge density and surface potential. The drift component (I_{drift}) of the drain current is significantly higher than the diffusion component in strong inversion region and rapidly vanishes in the sub-threshold region. Here, we have chosen $I_{drift} = I_{diffusion}$ as a point of threshold condition [14]. To calculate threshold voltage, we need (i) inversion charge density at threshold condition (i.e, $V_{fg} = V_{th}$ when $I_{drift} = I_{diffusion}$) (ii) front surface potential at threshold condition. By ignoring the backside inversion condition, we get total inversion charge density at threshold [15] as follows:

$$I_{ds} = I_{drift} + I_{diff} = -W.\mu\left(Q_{in}\frac{\partial\psi_s}{\partial x} + V_t\frac{\partial Q_{in}}{\partial x}\right) \quad (4)$$

By equating the drift component and diffusion component of I_{ds} i.e. -$Q_{in}\frac{\partial\psi_s}{\partial x} = V_t\frac{\partial Q_{in}}{\partial x}$, we get threshold condition as

$$Q_{in}@V_{th} = Q_{th} = C_{oxf}V_t \quad (5)$$

where $V_t = \frac{kT}{q}$ is the thermal volatge. To calculate front surface potential at threshold condition (ψ_{th}) we have solved (3) by Halley's method. The initial guess is derived using (1) after ignoring the back gate electric field E_{s2} as follows:

$$Q_{in} = \sqrt{2N_c kT exp\left(\frac{q(\psi_{s1} - V_{ch})}{kT}\right)} \quad (6)$$

$$\psi_{s1}^0 = \frac{kT}{q}\ln\frac{Q_{th}^2}{2N_c kT} + V_{ch} \quad (7)$$

As long as the back surface does not enter into inversion, we can express Q_{in} based on Gauss law as follows [13]:

$$Q_{in} = C_{oxf}\left(V_{fg}^* - \psi_{s1}\right) + \frac{C_{oxb}C_{si}}{C_{oxb} + C_{si}}\left(V_{bg}^* - \psi_{s1}\right) \quad (8)$$

where V_{fg}^* = V_{fg}-$\Delta\phi_1$, V_{fg} is front gate voltage and $\Delta\phi_1$ is front gate work function. After putting Q_{th} and ψ_{th} in (8), we get expression for front gate threshold voltage for long channel length device as:

$$V_{th,long} = \frac{Q_{th}}{C_{oxf}} + \Delta\phi_1 + \psi_{th} - \frac{C_{oxb}C_{si}}{C_{oxf}(C_{oxb} + C_{si})}\left(V_{bg}^* - \psi_{th}\right) \quad (9)$$

For short channel threshold voltage, we need to include drain induced barrier lowering (DIBL), vertical non-uniform doping (VNUD), back-bias shift [7], whose models are already included in the BSIM-IMG model. Threshold voltage expression for short channel devices is as follows:

$$V_{th,short} = V_{th,long} - \Delta V_{th,shift} \quad (10)$$

where $\Delta V_{th,shift}$ contains all the above effects.

III. Results and Discussion

There are some common methods available in literature to measure the threshold voltage quickly from measured drain current [15], [17]–[21] and capacitance characteristics [22]. In this section we have shown comparison of our model with the extraction techniques which extract the threshold voltage from measured drain current versus gate voltage characteristic. The threshold voltage extraction techniques used in this work are as follows: (i) The CC method [17] calculates the threshold voltage as the gate voltage at which current reaches to a given arbitrary constant value. $I_{ds} = I_0\frac{W}{L}$ where W and L are effective channel width and length respectively and I_0 is constant current chosen arbitrarily. (ii) The ELR method is used to calculate the threshold voltage in the linear region [18] and calculates the threshold voltage by finding the gate-voltage axis intercept of the linear extrapolation of the I_{ds} vs. V_{gs} curve at its maximum first derivative point. But this method is not reliable as maximum slope point gets shifted by mobility degradation and parasitic series resistances. (iii) The

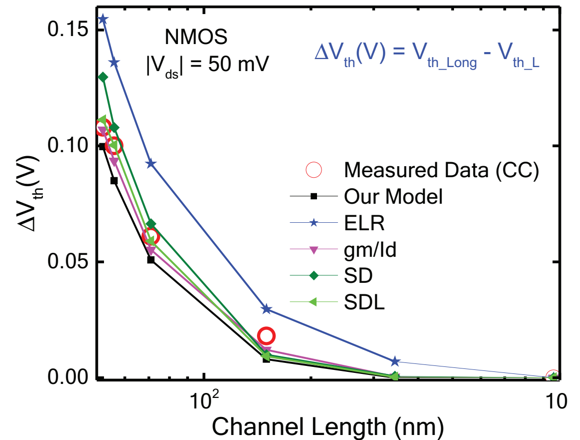

Fig. 2. ΔV_{th} vs length characteristic for n-channel FDSOI transistors at $|V_{ds}|$ = 50 mV and V_{bg} = 0 V. The channel length is varied from 52 nm to 961 nm. Threshold voltage extracted from methods g_m/I_d, ELR, ERS, SD and SDL are simulated using current-voltage (I-V) characteristics of the BSIM-IMG model while CC method (I_0 = 200 nA) is used to extract threshold voltage from the measured data provided by LEAP, Japan [16].

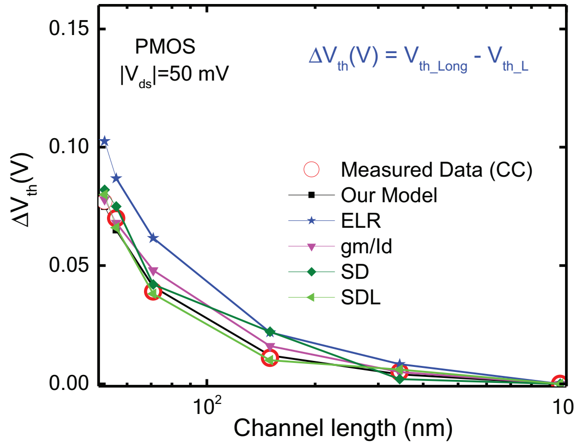

Fig. 3. ΔV_{th} vs length characteristic for p-channel FDSOI transistors at $|V_{ds}|$ = 50 mV and V_{bg} = 0 V. The channel length is varied from 52 nm to 961 nm. Measured data is from LEAP Japan's FDSOI technology [16].

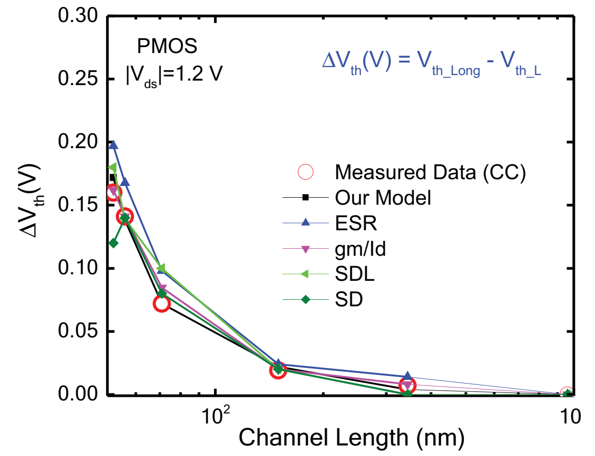

Fig. 5. ΔV_{th} vs length characteristic for p-channel FDSOI transistors at $|V_{ds}|$ = 1.2 V and V_{bg}= 0 V. The channel length is varied from 52 nm to 961 nm. Measured data is from LEAP Japan's FDSOI technology [16].

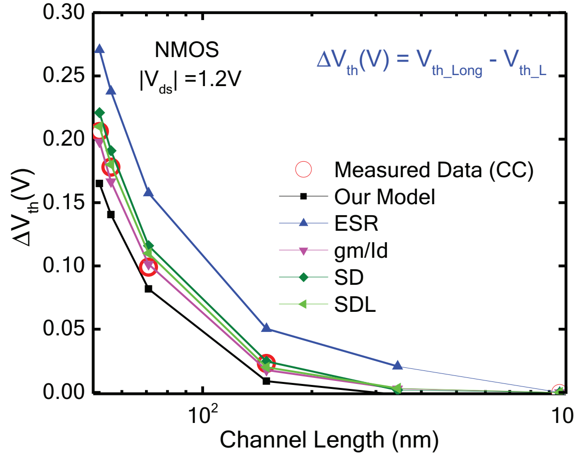

Fig. 4. ΔV_{th} vs length characteristic for n-channel FDSOI transistors at $|V_{ds}|$ = 1.2 V and V_{bg}= 0 V. The channel length is varied from 52 nm to 961 nm. Measured data is from LEAP Japan's FDSOI technology [16].

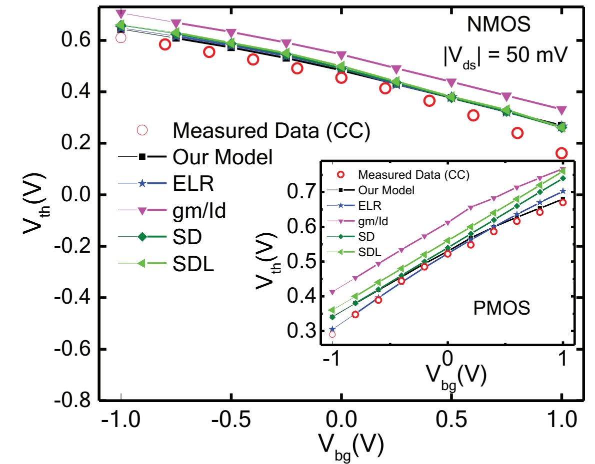

Fig. 6. The threshold voltage vs back gate bias characteristic for n-channel and p-channel FDSOI transistors at $|V_{ds}|$ = 50 mV. Model has captured back-bias impact very well in linear region. The variation of V_{th} is not exactly linear due to substrate depletion effect [7]. Measured data for channel length L_g = 52 nm is from LEAP Japan's FDSOI technology [16].

ESR method is famous for calculating the threshold voltage in the saturation region [19] and calculates the threshold voltage by finding the gate voltage axis intercept of the $\sqrt{I_{ds}}$ vs. V_{gs} characteristic linearly extrapolated at its maximum first derivative point. (iv) The g_m/I_{ds} method [15] defines the threshold voltage as the gate volatge at which g_m/I_{ds}=0.5$g_m/I_{ds}\ |max$. (v) The Second-derivative (SD) method [20] is proposed to avoid the dependence on the series resistances, it determines threshold voltage as the gate voltage at which the derivative of the trans-conductance is maximum. (vi) Second derivative logarithmic (SDL) method [21] defines the threshold voltage as the gate voltage at which the second derivative of the logarithm of the drain current takes on a minimum value.

We have first extracted global DC parameter set by fitting static characteristics [7] for channel lengths 961 nm to 52 nm. Then this parameter set is used to obtain V_{th} from various methods. Fig. 2 to 5 show that model ΔV_{th} results are in close agreements with the other extracted ΔV_{th} from different methods. Here ΔV_{th} at any channel length (L) is calculated as the difference between long channel threshold voltage ($V_{th-Long}$) and threshold voltage at the same channel length (V_{th-L}). CC method is used to extract threshold voltage from the measured data provided by LEAP, Japan [16]. The drain voltage for linear region operation is 50 mV and for saturation region is 1.2 V. Fig. 2 and Fig. 3 show the variation of threshold voltage with channel length at V_{bg} = 0V for the linear region which shows the ability of our model to capture the threshold voltage across lengths for NMOS and PMOS both. Fig. 4 and Fig. 5 show the variation of threshold voltage with channel length at V_{bg} = 0 V for saturation region operation. It is clear from Fig. 2 to Fig. 5 that the threshold voltage becomes lower for $|V_{ds}|$ = 1.2 V in comparison to the

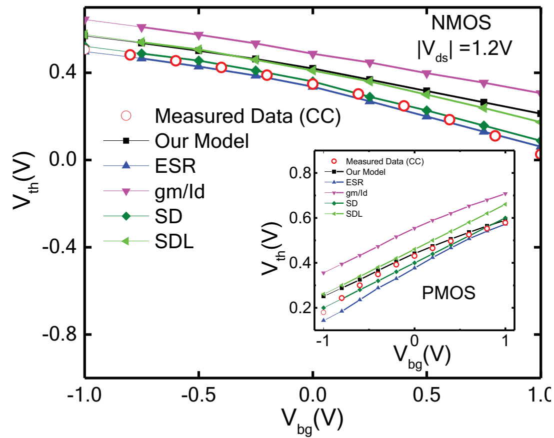

Fig. 7. The threshold voltage vs back gate bias characteristic for n-channel and p-channel FDSOI transistors at $|V_{ds}|$ = 1.2 V. Model has captured back-bias impact very well in saturation region. The variation of V_{th} is not exactly linear due to substrate depletion effect [7]. Measured data for channel length L_g = 52 nm is from LEAP Japan's FDSOI technology [16].

threshold voltage at $|V_{\rm ds}|$ = 0.05 V due to drain induced barrier lowering effect.

Fig. 6 and Fig. 7 show the variation of threshold voltage with back gate bias for linear and saturation regions respectively. For NMOS device, in the condition of reverse back-bias $V_{\rm bg}$ = -1 V, inversion get delayed due to depletion at the back-interface, as a result the threshold voltage of the device increases in comparison to zero back-bias ($V_{\rm bg}$ = 0 V) and vice versa for PMOS device. Whereas in the case of forward back-bias ($V_{\rm bg}$ = 1 V) in NMOS device, inversion comes earlier in comparison to zero back bias ($V_{\rm bg}$ = 0 V), as a result the threshold voltage of the device decreases and vice versa for PMOS device. Fig. 6 and 7 show that V_{th} vs. V_{bg} characteristic is not exactly linear. This non-linear behavior in threshold voltage with back-bias is coming due to substrate depletion effect [7]. As some fraction of the applied back-gate bias drops in the substrate region and creates depletion in the substrate which changes the threshold voltage of the device. Thus Fig. 6 and 7 show that the model accurately captures the substrate depletion effect.

IV. Conclusion

A new formulation of threshold voltage using the BSIM-IMG model is presented. The model accounts for real device effects and utilizes surface potential based core of the BSIM-IMG compact model. The model captures threshold voltage across lengths, drain and back-biases and shows excellent agreement with experimental data. The threshold voltage extracted from ERL and ERS methods has shown the good agreement with the proposed model which makes the model a suitable candidate for the circuit designers.

V. Acknowledgement

This work was supported in part by Semiconductor Research Corporation, in part by Science and Engineering Research Board (SERB), in part by Ramanujan Fellowship and in part by Council of Scientific and Industrial Research (CSIR).

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