Predictive Effective Mobility Model for FDSOI Transistors using Technology Parameters

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***Abstract*—The formulation of effective mobility for fully depleted silicon-on-insulator (FDSOI) transistors is a very challenging task. As vertical electric field (E_{eff}) changes it's sign from positive to negative according to the front and back channel dominance which results in non-unique relationship between E_{eff} and carrier distribution. This is the first time, when a predictive mobility model for wide range of back gate biases, solely dependent on technology parameters (front and back gate oxide thickness $T_{ox/box}$, threshold voltage V_{th}, front/back gate bias $V_{fg/bg}$ and flat-band voltage V_{fb}) is proposed. This predictive mobility model allows the user to predict the deviation in device characteristics due to the variations in the device structure.**

***Index Terms*—FDSOI, Model, Split-CV, Mobility.**

I. Introduction

Below 20 nm technology node, bulk transistors are facing challenges like severe short channel effects, random dopant fluctuation etc [1]. Different architectures like fully depleted silicon on insulator (FDSOI) [2] and FinFETs [3] are introduced to drive the CMOS market further for meeting high performance and low power demands. Due to the presence of ultra thin buried oxide layer (BOX), FDSOI transistor has threshold voltage tuning facility by back gate biasing [4]–[7] in comparison to FinFET transistors. This also results in strong front and back gate coupling which makes the effective electric field [8] and inversion layer mobility [9] calculations difficult in FDSOI transistors as compared to bulk transistors.

In bulk transistor, the inversion layer mobility follows a universal relation and is independent of substrate bias, the substrate doping and oxide thickness when plotted against effective transverse electric field $E_{eff(bulk)}$ [10],

$$E_{eff(bulk)} = \frac{Q_{dep} + \eta Q_{inv}}{\epsilon_{Si}} \quad (1)$$

where Q_{dep}, Q_{inv} are the depletion and inversion charges respectively, ϵ_{Si} is the relative permittivity of silicon and η is 1/2 for nMOS and 1/3 for pMOS transistors. This universal mobility curve (UMC) is considered as a reference curve to compare any new technology and is very useful to understand the MOS transistor physics [8].

Unfortunately, the same definition of $E_{eff(bulk)}$ is not applicable to the FDSOI transistors because electric field at the back interface (E_{sb}) is not always equal to zero as in bulk MOS transistor [11]. This had led to lots of discussion on the non-universality of mobility in literature [8], [12], highlighting the importance of E_{sb}. To account the impact of E_{sb} on mobility, the models proposed till date [13]–[15] have tried to include back gate electric field E_{sb} along with the front-gate electric field E_{sf} which results in effective electric field $E_{eff} = \frac{Q_b + \eta Q_{inv}}{\epsilon_{Si}} + E_{sb}$. Unfortunately, the lumped parameter E_{eff} is not a convenient quantity to use, when expressed in terms of Q_b and Q_{inv} [11], [15] as their measurements are difficult [16]. In this work, we have proposed a complete technology parameter based compact model for E_{eff} and effective mobility μ_{eff}. Due to some manufacturing variations, technology parameters ($T_{ox/box}$, V_{th}, $V_{fg/bg}$, V_{fb}) show slight device to device variations. Also devices fabricated using different processes have different technology parameters. All these result in deviation of mobility and hence the device characteristics. The proposed predictive model captures these variations and predicts the effective mobility for wide range of back bias.

This paper is organized as follows. The mobility and threshold voltage extraction are explained in Section II. The proposed effective mobility model is discussed in Section III. Model validation is discussed in Section IV followed by conclusion in Section V.

II. Mobility and Threshold Voltage Extraction

FDSOI devices from CEA-LETI were used for C-V and I-V measurements. The device chosen for this work has dimensions: channel length L_g = 10 μm, channel width W_g = 50 μm and front-gate oxide thickness T_{ox} = 1.2 nm, back gate oxide thickness T_{box} = 25 nm and silicon channel thickness T_{Si} = 8 nm. I-V and C-V measurements are done using Keysights B1500A semiconductor device parameter analyzer. I-V measurements are done at drain voltage (V_{ds}) = 10 mV while C-V measurements are done at V_{ds} = 0 V.

A. Mobility Extraction by Split-CV method

Fig. 1(a) shows the variation in gate to channel capacitance (C_{gc}) as a function of V_{fg} for different V_{bg}. For high positive V_{bg} (i.e., Region-I), there is a plateau in C_{gc} - V_{fg} characteristic. This plateau indicates the formation of inversion layer at back side channel while there is no channel formed yet at the front interface [17], [18]. In region II, the front gate voltage

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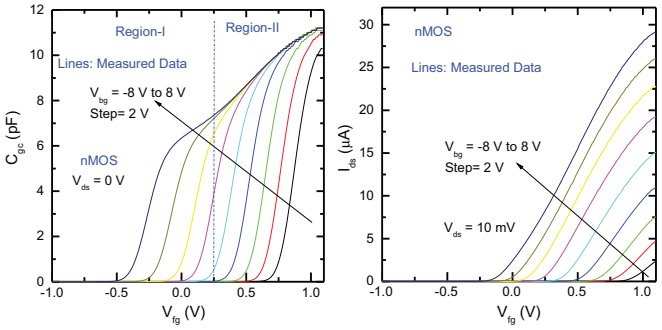

Fig. 1. The impact of back gate bias on measured C_{gc} and I_{ds} is illustrated. (a) C_{gc} vs V_{fg} characteristic. (b) I_{ds} vs V_{fg} characteristic. Back gate bias V_{bg} sweeps from -8 to 8 V with the step size of 2 V. Device dimensions are: L_g = 10 μm, W_g = 50 μm, T_{ox} = 1.2 nm, T_{box} = 25 nm, T_{Si} = 8 nm. All lines are showing measurement data.

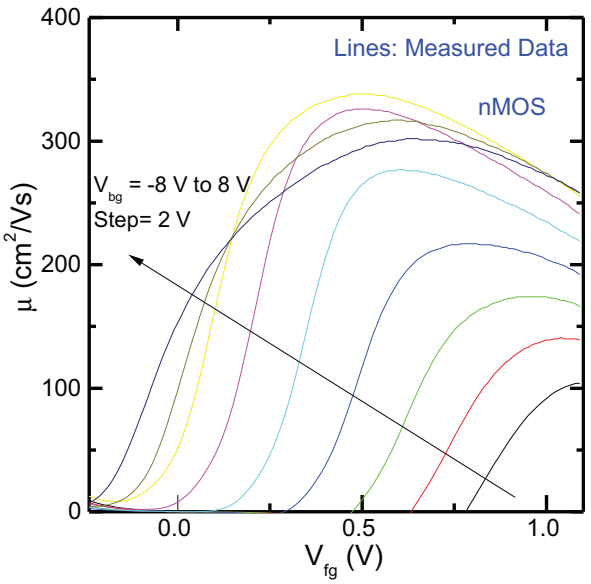

Fig. 2. Mobility μ vs V_{fg} curve, by using definition (2). Device dimensions are: L_g = 10 μm, W_g = 50 μm, T_{ox} = 1.2 nm, T_{box} = 25 nm, T_{Si} = 8 nm. All lines are showing measurement data.

is high, which results in coexistence of front as well as back channel inversion [19]. Fig. 1(b) shows the variation in drain current I_{ds} with V_{fg} for different V_{bg}. As V_{bg} increases, V_{th} of device decreases which results in high I_{ds} while with negative V_{bg}, inversion gets delayed and result in reduced I_{ds} [20].

The split C-V method is widely used for determining the mobility, because it estimates carrier density accurately [10]. Using this approach, the channel mobility is extracted using the C_{gc} vs V_{fg} characteristic and drain current measurements at different back gate biases [17] as follows

$$\mu = \frac{L_{eff} I_{ds}}{W_{eff} Q_{inv} V_{ds}} \tag{2}$$

where W_{eff}, L_{eff} are the channel width and length respectively and C_{ox} is front gate oxide capacitance. Q_{inv} is the charge per unit area which is obtained by integrating the measured C_{gc} - V_{fg} characteristic.

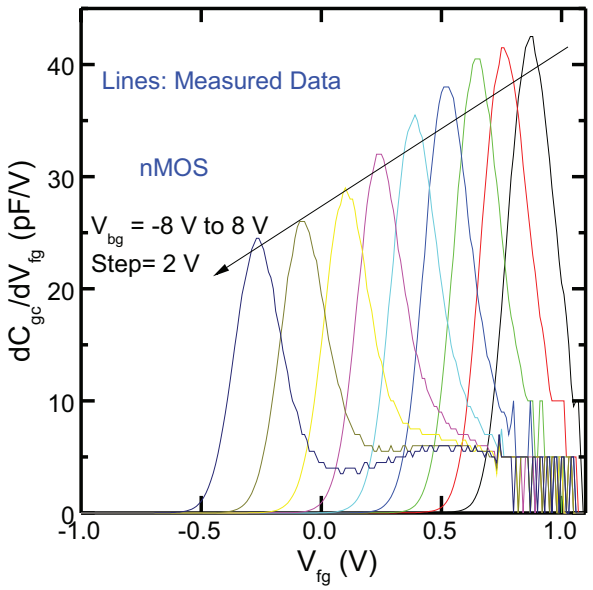

Fig. 3. $\frac{dC_{gc}}{dV_{fg}}$ vs V_{fg} for different V_{bg} is illustrated. Device dimensions are: L_g = 10 μm, W_g = 50 μm, T_{ox} = 1.2 nm, T_{box} = 25 nm, T_{Si} = 8 nm. All lines are showing measurement data.

To neglect the effect of horizontal electric field on channel mobility, the measurements were carried out at V_{ds} = 10 mV. Also the mobility curves were corrected for access resistance R_{access} = 2*103 $\Omega.\mu$m, calculated using R_{on}(L) method [21]. The corrected mobility curves show that the R_{access} has negligible effect due to the use of long channel length device. The extracted μ vs V_{fg} characteristic for different back gate bias are shown in Fig 2.

B. Threshold Voltage Extraction

Fig. 1(b) shows that back-gate bias has a significant influence on V_{th}, thus it is important to extract V_{th} accurately. There are several methods available in literature to extract threshold voltage of MOS transistors [22], [23]. The derivative of the gate to channel capacitance method (see Fig 3) gives much better resolution in channel separation, because it is less sensitive to series resistance as compared to the current measurements. Extracted threshold voltage from the peak of $\frac{dC_{gc}}{dV_{fg}}$ curve is shown in Fig 4.

III. Proposed Effective Mobility Model

In a FDSOI transistor, the two boundary conditions from Gauss law at front and back gates are given as

$$\epsilon_{si} E_{sf} = Q_f = \frac{\epsilon_{ox}}{T_{ox}} (V_{fg} - V_{fb1} - \psi_1) \tag{3}$$

$$\epsilon_{si} E_{sb} = Q_b = \frac{\epsilon_{ox}}{T_{box}} (V_{bg} - V_{fb2} - \psi_2) \tag{4}$$

where Q_f and Q_b are the front/back gate charges and ϵ_{si} and ϵ_{ox} are the silicon and oxide material permittivity, respectively.

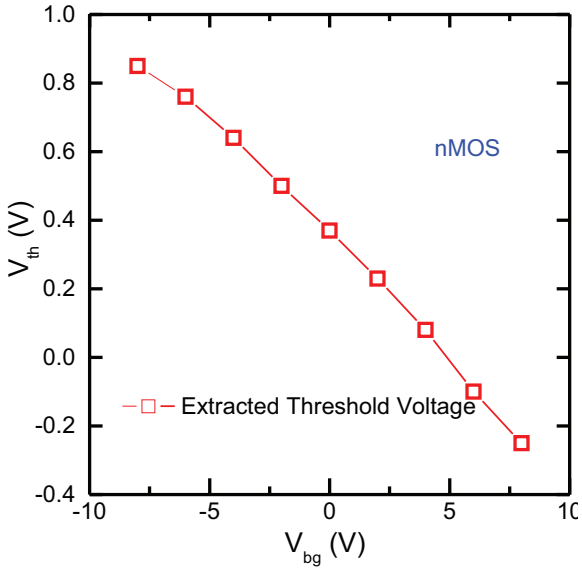

Fig. 4. V_{th} vs V_{bg} curve extracted from $\frac{dC_{gc}}{dV_{fg}}$ vs V_{fg} characteristic. Device dimensions are: L_g = 10 μm, W_g = 50 μm, T_{ox} = 1.2 nm, T_{box} = 25 nm, T_{Si} = 8 nm.

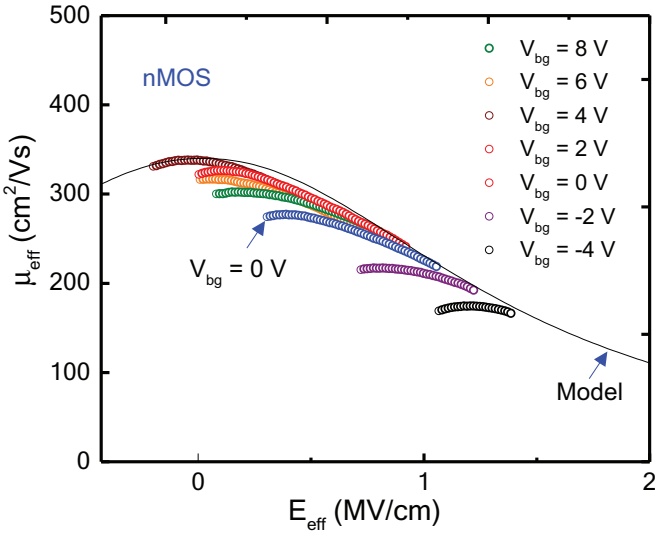

Fig. 5. μ_{eff} vs E_{eff} behavior of FDSOI transistor is illustrated. Here, α = 0.72 and β = 1.1, **U0** = 380 cm^2/Vs, **UA** = 0.83 cm/MV and **EU** = 1.85. Device dimensions are: L_g = 10 μm, W_g = 50 μm, T_{ox} = 1.2 nm, T_{box} = 25 nm, T_{Si} = 8 nm. Black solid line: Predictive Model, Symbols: Measurement Data.

V_{fb1} and V_{fb2} are the flat band voltages, T_{ox} and T_{box} are the oxide thicknesses at front and back gates, respectively. E_{sf} and E_{sb} are the surface electric fields and ψ_1 and ψ_2 are the surface potentials at front and back gates, respectively.

$$E_{sf} = \frac{V_{fg} - V_{fb1} - \psi_1}{3T_{ox}} \tag{5}$$

$$E_{sb} = \frac{V_{bg} - V_{fb2} - \psi_2}{3T_{box}} \tag{6}$$

We have assumed $\psi_1 = \psi_2 = 2\phi_f$ i.e., threshold condition, where ϕ_f is the Fermi potential. Effective mobility (μ_{eff}) can be expressed as a function of E_{eff} (i.e., average of front and back surface electric fields). Using (5) and (6), E_{eff} becomes

$$\begin{aligned} E_{eff} &= \frac{1}{6T_{ox}}\left[(V_{fg} - V_{fb} - 2\phi_f) - \frac{T_{ox}}{T_{box}}(V_{bg} - V_{fb} - 2\phi_f)\right] \\ &= \frac{1}{6T_{ox}}\left[V_{fg} - \frac{T_{ox}}{T_{box}}V_{bg} - \left(1 - \frac{T_{ox}}{T_{box}}\right)(V_{fb} + 2\phi_f)\right] \end{aligned} \tag{7}$$

where $V_{fb1} = V_{fb2} = V_{fb}$ for derivation simplicity. In thin BOX FDSOI transistors, the technological variations at the back interface like oxide thickness, interface quality and work-function plays an important role. We have expressed V_{bg} in terms of threshold voltage V_{th} which automatically captures all these process variations in our model [24]. This relation also helps in capturing the effect of back bias on carrier distribution which makes effective mobility curves, nearly independent of back gate bias. As shown in Fig. 4, V_{th} can be expressed as

$$V_{th} = -\mathbf{m}V_{bg} + V_{th0} \tag{8}$$

where **m** is representing the slope and V_{th0} is the threshold voltage at zero back gate bias. By incorporating (8) in (7), we get final expression for E_{eff} as,

$$\begin{aligned} E_{eff} &= \frac{1}{6T_{ox}}\left[V_{fg} + \frac{T_{ox}}{mT_{box}}V_{th}^{'} - \left(1 - \frac{T_{ox}}{T_{box}}\right)(V_{fb} + 2\phi_f)\right] \\ &= \frac{1}{6T_{ox}}\left[V_{fg} + \alpha V_{th}^{'} - \beta(V_{fb} + 2\phi_f)\right] \end{aligned} \tag{9}$$

where $V_{th}^{'}$ = $|V_{th}|$ - V_{th0} and $\alpha = \frac{T_{ox}}{mT_{box}}$, $\beta = \left(1 - \frac{T_{ox}}{T_{box}}\right)$. Here, α and β are taken as model parameters. To account for different V_{fb1} and V_{fb2} conditions, β can be tuned further.

IV. Model Validation

The results for mobility discussed in Section II plotted by our proposed model are shown in Fig 5. E_{eff} is negative for $V_{bg} > 0$ V and as V_{fg} increases, the charge centroid shifts from the back interface to the front interface and E_{eff} changes it's sign from negative to positive. In strong inversion region, the effective mobility curves are converging into the single curve. This single mobility curve is predicted using our effective mobility model where μ_{eff} is a function of proposed E_{eff} as (10). The solid black line shown in Fig 5 is predicting the effective mobility behavior for different back bias.

$$\mu_{eff} = \frac{\mathbf{U0}}{1 + \mathbf{UA} \cdot |E_{eff}|^{\mathbf{EU}}} \tag{10}$$

where E_{eff} is electric field in MV/cm. **U0** is low field mobility parameter while **UA** and **EU** parameters are used to capture surface roughness scattering [25]. When amount of inversion charge is lower in the channel, mobility gets limited by coulomb scattering [26]. Note that our model does not consider the coulomb scattering.

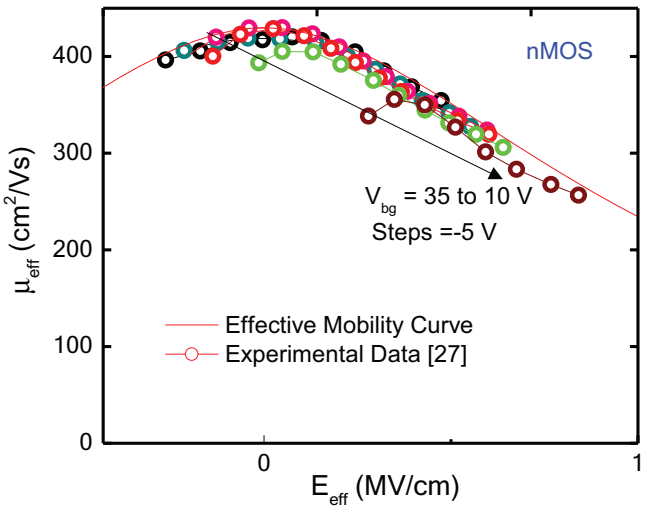

Fig. 6. μ_{eff} vs E_{eff} behavior of FDSOI transistor. Device dimensions are: L_g = 10 μm, W_g = 10 μm, T_{ox} = 1.75 nm, T_{box} = 145 nm, T_{Si} = 11 nm. Red solid line: Predictive Model, Symbols: Experimental Data [27].

To check the model validity for FDSOI transistors with different set of technology parameters (T_{ox}, T_{box} and T_{si}), we have plotted proposed μ_{eff} vs E_{eff} for the experimental data obtained from [27]. The model shows good agreement for this thick BOX FDSOI transistor for a wide range of back bias as shown in Fig 6. The proposed model is able to predict the mobility for differently processed FDSOI transistors as shown in Fig 5 and Fig 6. These results also show that the inclusion of threshold voltage in our model makes mobility curves independent of back bias.

V. Conclusion

The predictive mobility model for FDSOI transistors is presented for a wide range of back gate bias. Model has shown good agreement with the measured data obtained from CEA-LETI as well as with the data reported earlier in literature. The novelty in the proposed model is its dependency, solely on technology parameters which are monitored daily in the practical engineering world by circuit designers.

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