Compact Models of Negative-Capacitance FinFETs: lumped and distributed charge models

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***Abstract*—This work presents insights into the device physics and behaviors of ferroelectric based negative capacitance FinFETs (NC-FinFETs) by proposing lumped and distributed compact models for its simulation. NC-FinFET may have a floating metal between ferroelectric (FE) and the dielectric layers and the lumped charge model represents such a device. For a NC-FinFET without a floating metal, the distributed charge model should be used and at each point in the channel the ferroelectric layer will impact the local channel charge. This distributed effect has important implications on device characteristics as shown in this paper. The proposed compact models have been implemented in circuit simulators for exploring circuits based on NC-FinFET technology.**

I. Introduction

Negative capacitance FETs (fig. 1) are quickly emerging as promising devices to achieve sub-60 mV/decade sub-threshold slope and high I_{on} [1], [2]. With recent experimental demonstrations of FE based NC-FETs [3], [4], there is an urgent need for analysis of device operation and circuit performance via compact models. In our previous work [5], we presented a lumped charge model NC-FinFETs. In this work we derive new insights into the device operation by analyzing and modeling both devices with floating metal gate and without it. The distributed charge model needs to be used for device without the floating metal. Significant differences in the characteristics of these two types of NC-FinFETs will be presented .

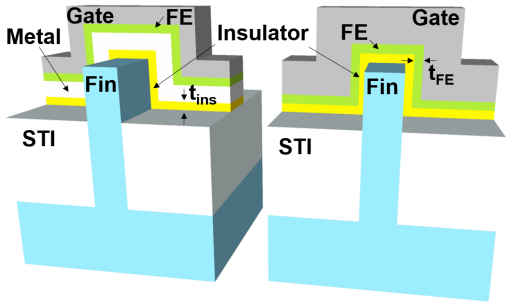

Fig. 1: Schematic of NC-FinFETs. Lumped NC-FinFET (left) has a floating gate between insulator and FE. The distributed NC-FET (right) does not have a floating gate.

II. Unified Compact Model

The unified compact model, BSIM-CMG accurately predicts the charge and current voltage characteristics of different FinFETs and gate-all-around structures [6]. BSIM-CMG's core equation is a single unified charge model (UCM), a closed form relationship between the mobile charge (Q_m) and the applied terminal voltages (V_G,V_D,V_S,V_B) given in a normalized form as follows:

$$v_G - v_o - v_{ch} = -q_m + \ln(-q_m) + \ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) \quad (1)$$

where v_{ch} is the normalized channel potential. v_o and q_t are defined in table I.The UCM requires only four different model parameters [6]: insulator capacitance (C_{ins}), channel area (A_{ch}), channel doping (N_{ch}) and effective channel width (W_{eff}). Using these parameters, we accurately modeled the characteristics of a 14nm node Ultra-Low-Power FinFET [7], which is the baseline FinFET technology used in this work.

TABLE I: Unified compact model and FE model variables

Variable	Definition
v_G, v_{ch}, v_T	$\frac{V_G}{v_T}$, $\frac{V_{ch}}{v_T}$, $\frac{kT}{q}$ (Thermal Voltage)
q_m, q_{dep}	$\frac{Q_m}{v_T C_{ins}}$, $\frac{-qN_{ch}A_{ch}}{v_T C_{ins}}$
v_o	$v_{FB} - q_{dep} - \ln\left(\frac{2qn_i^2 A_{ch}}{v_T C_{ins} N_{ch}}\right)$
q_t	$(q_m + q_{dep})r_N$
r_N	$\frac{A_{Fin}C_{ins}}{\varepsilon_{ch}W_{eff}^2}$
a_0	$2\alpha t_{FE} C_{ins}/W_{eff}$
b_0	$4\beta t_{FE}(v_T C_{ins}/W_{eff})^3/v_T$
c_0	$6\gamma t_{FE}(v_T C_{ins}/W_{eff})^5/v_T$

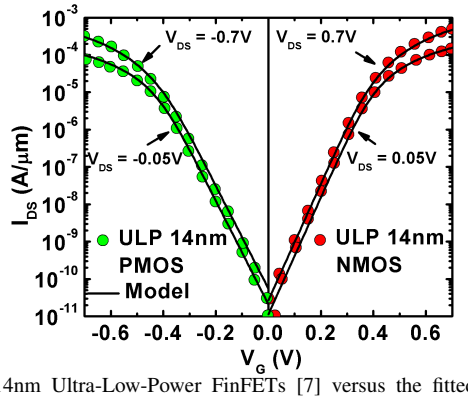

Fig. 2: 14nm Ultra-Low-Power FinFETs [7] versus the fitted BSIM-CMG Model.

III. Ferroelectric Material Model

A compact model of FE materials, which captures the negative capacitance correctly, is obtained using the Landau Khalatnikov (LK) equation [8]. LK expresses the relationship between electric-field (E) and polarization (P) of a FE:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \quad (2)$$

where α, β, and γ, are material parameters. Equation (2) captures the energetically unstable region where the capacitance is

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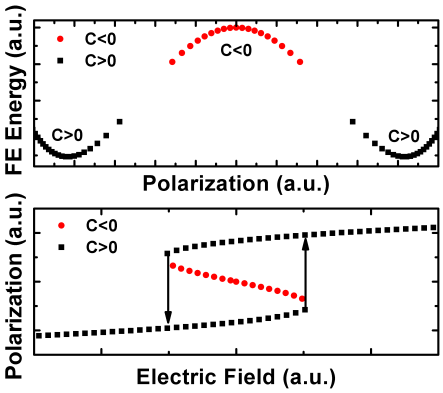

Fig. 3: Energy landscape and polarization of the FE with red dots showing the negative capacitance regime.

negative (red dots in fig. 3). The negative capacitance regime of FE materials can be stabilized by connecting it in series with a positive capacitance [1] such as the gate capacitance of the FinFET in the FE NC-FinFET system. The charges in the two series capacitors are equal, i.e., $P = L_G Q_{ch}$, where Q_{ch} is the channel (dopant and mobile) charge per unit length. It is therefore possible to model such a system replacing v_G in (1) with $v_G - v_{FE}$ where v_{FE} is the normalized FE voltage from (2):

$$v_{FE} = -(a_0 q_{ch} + b_0 q_{ch}^3 + c_0 q_{ch}^5) \tag{3}$$

where a_0, b_0, and c_0 are defined in table I. The model simulates the behavior of the $V_{DS} = 0V$ NC-FinFET connection (figs. 4 and 5). The compact model captures how the FE thickness (t_{FE}) can be used to stabilize the negative capacitance (avoiding the hysteresis by making $-C_{FE} > C_{mos}$), and to adjust the voltage gain, which is $|C_{FE}|/(|C_{FE}|-C_{mos})$ [2]. The concept of voltage amplification is illustrated in Fig. 5. Because V_{FE} is negative, the voltage across C_{mos} in Figs. 4 and 5 is larger than V_G. This is the gist of why NCFET can operate at lower voltage. There is no significant voltage gain unless C_{mos} is comparable to $-C_{FE}$.

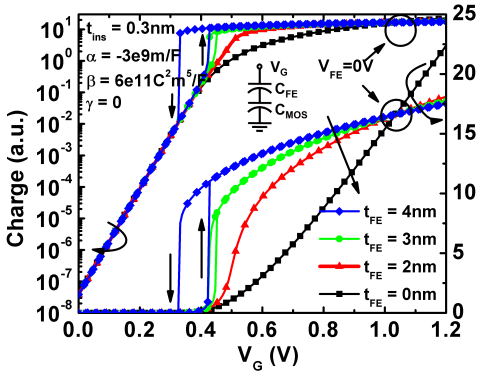

Fig. 4: Channel charge versus V_G for different t_{FE} obtained from the model. Note that all curves meet at a given V_G where $V_{FE} = 0V$ (see fig. 5). $C_{parasitic} = 0$ in Figs. 4 to 7.

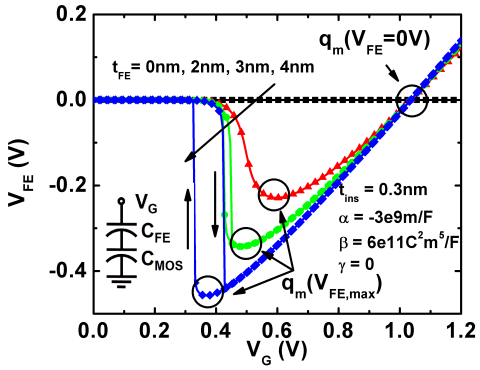

Fig. 5: V_{FE} versus V_G for different t_{FE} obtained from the model. At $V_{FE} = 0V$, $q_m = -(-a_0/b_0)^{0.5}$. V_{FE} peak is obtained at $q_{m,V_{FEPEAK}} = -(-a_0/(3b_0))^{0.5}$, making $V_{FE,max}$ linearly dependent on t_{FE}.

IV. Lumped NC-FinFET Model

In a NC FinFET with a floating metal gate, the charge used to calculate v_{FE} is the average charge in the gate:

$$q_G = \frac{1}{L_G}\int_0^{L_G} (q_m + q_{dep} + q_{parasitics})dx \tag{4}$$

$v_G - v_{FE}$ is the voltage of the floating gate, i.e., the gate of the underlying FinFET. Since calculating q_G requires q_m, it and q_G cannot be obtained explicitly using (1) and (4); therefore, they are calculated self-consistently by the simulator using an internal model node for the floating gate [5]. The normalized current can be calculated as in a regular FinFET [6]:

$$i_{DS} = \int_0^{v_{DS}} q_m dv_{ch} \tag{5}$$

Figs. 6 and 7 show the current-voltage and FE voltage simulated characteristics of lumped FE NC-FinFETs for different t_{FE} values. Drain current is amplified when a FE layer is used. The current amplification is proportionally to t_{FE} for V_G values close to threshold voltage. When t_{FE} is too thick, the device is no longer stable and there is an anticlockwise hysteresis present in the current.

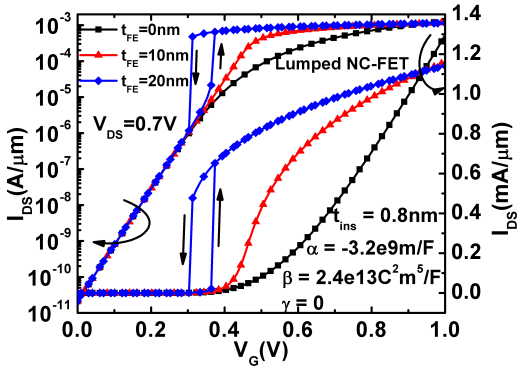

Fig. 6: Lumped model generated $I - V$ of NC-FinFETs for several t_{FE}. Anticlockwise hysterisis is present for FE NC-FinFET with overly large t_{FE}.

Figs. 8 and 9 show the current-voltage and FE voltage characteristics of the lumped NC-FinFETs for different parasitic capacitance values. The parasitic capacitances increase the charge available in the subthreshold region, producing a boost

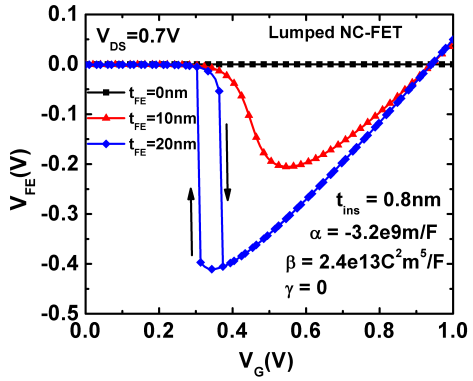

Fig. 7: Modeled V_{FE} versus V_G of lumped NC-FinFETs for different t_{FE}. For $t_{FE} = 10nm$ the FE is not stabilized, producing anticlockwise hysteresis.

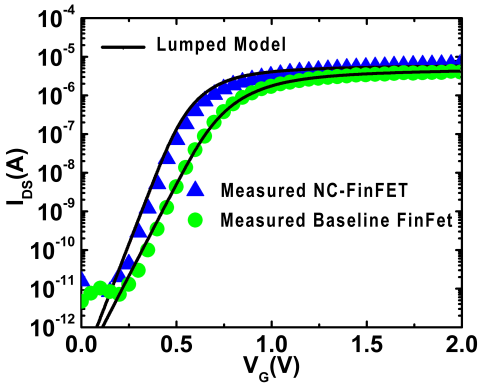

Fig. 10: Experimental validation of the lumped model against FE NC-FinFET [3], [5].

in the voltage amplification before onset of inversion (fig. 9). The model has been validated against experimental data obtained from a NC-FinFET with excellent agreement (fig. 10) [5].

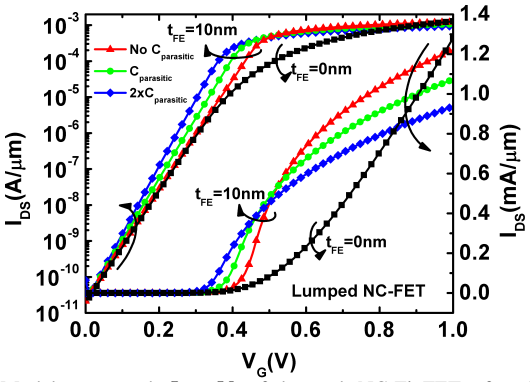

Fig. 8: Model generated $I - V$ of lumped NC-FinFETs for different $C_{parasitic}$. The larger C_{mos} increase the voltage gain in the subthreshold region.

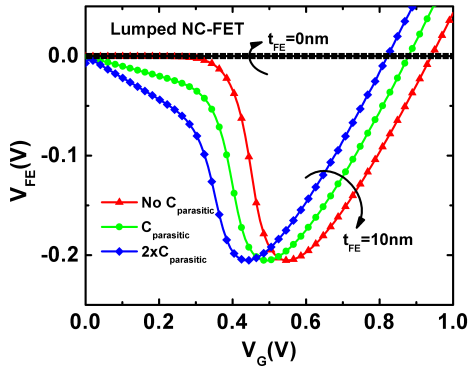

Fig. 9: Model generated V_{FE} versus V_G of lumped NC-FinFETs for different $C_{parasitic}$. Note that the peak magnitude of V_{FE} is not affected.

V. Distributed NC-FinFET Model

Equation (1) can be used to model NC-FinFETs without a floating gate by replacing v_G by $v_G - v_{FE}$ and using the local channel charge along the channel to determine the local v_{FE}. If the resulting system does not produce hysteresis characteristics, equation (5) can be used directly to obtain the drain current. When hysteresis is present, the drain current must be obtained considering the hysteresis at each point of the channel. This can be implemented using Gauss-Legendre quadrature:

$$i_{DS} = \int_0^{v_{DS}} q_m dv_{ch} \approx \sum_{i=1}^{n} q_m(v_{ch,i}) w_i \qquad (6)$$

where $v_{ch,i}$ is given by $v_{ch,i} = (v_D - v_S)(x_i + 1)/2 + v_S$, n represents the number of Gauss points used for the integration, and x_i and w_i are the abscissas and weights of the Gauss-Legendre quadrature. Fig. 11 shows the drain current versus gate voltage of distributed NC-FinFETs for different t_{FE} values. The FE material causes a current amplification; however, it is different than the case of a lumped configuration. Compared to the lumped configuration, the strong inversion current slop of the distributed device is not largely affected by t_{FE} thickness. In addition, the hysteresis transitions are smoother than the lumped case. The model captures this distributed nature of the device by evaluating the charge and V_{FE} along the channel length (fig. 12). Including parasitic capacitance also improves the subthreshold swing of the device for the same reason it does to the lumped configuration.

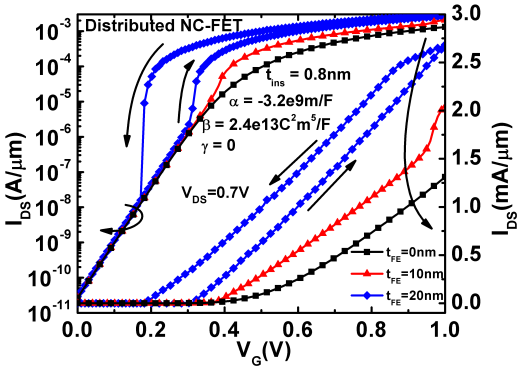

Fig. 11: Modeled $I - V$ of distributed NC-FinFETs for different t_{FE}. hysterisis is present overly large tFE but smoother than the case of lumped NC-finFET.

VI. Lumped versus Distributed NC-FinFETs

Fig. 13 shows a comparison of the drain current versus gate voltage in lumped and distributed device configurations. The

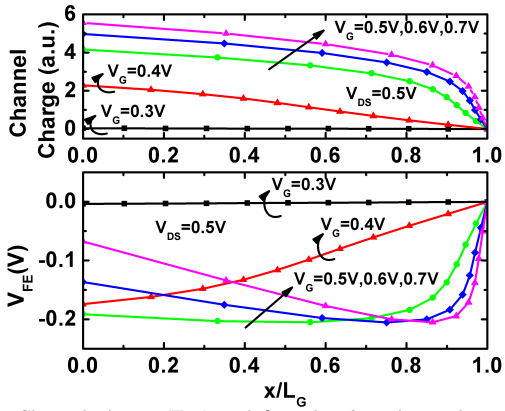

Fig. 12: Channel charge (Top) and ferroelectric voltage along the channel length for different gate voltages in the distruted charge NC-FinFET shown in fig. 11 with $t_{FE} = 10nm$.

subthreshold swing improvement is similar in both cases. On the other hand, the lumped device current becomes saturated at larger voltages, where the distributed configuration, shows an approximately linear increment of current for larger gate bias. The transconductance of lumped device has a larger peak than the distributed one (fig. 14); where the later has a transconductance with lower value but approximately constant at higher bias windows. The differences in device characteristics are attributed to the totally different FE voltage and charge distribution in the device.

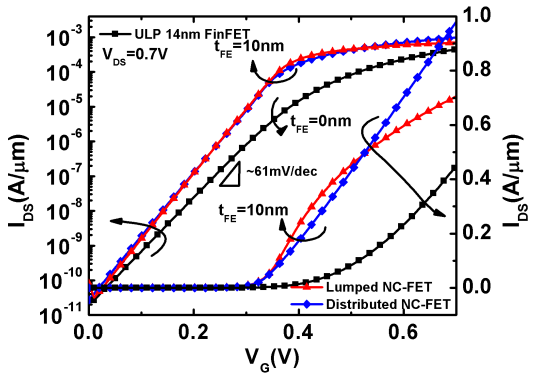

Fig. 13: $I-V$ lumped and distributed NC-FinFETs. Subthreshold behaviors are similiar; however, strong inversion characteristics are different.

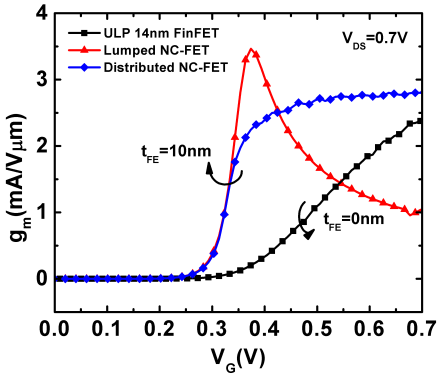

Fig. 14: Transconductance (g_m) versus gate voltage in lumped and distributed configurations. A larger larger g_m peak is presented in the lumped device compared to the distributed configuration; however, the larger peak rapidly decreases as V_G increases.

VII. Model Robustness

The robustness of the lumped model has been already verified in a commercial circuit simulator [5]. Here, the distributed model is implemented in Verolog-A code [9] and tested in a commercial circuit simulator. Fig. 15 shows the results of 17-stage ring-oscillator circuit simulations using the distributed charge model. Simulations converge in similar speed rates compare to BSIM-CMG model, validating the its functionality for IC simulation and design.

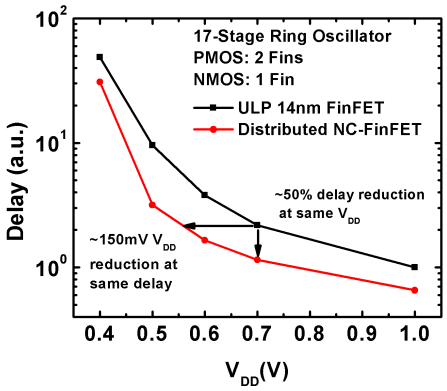

Fig. 15: Delay versus supply voltage of 17-stage ring-oscillator. This example shows the benefits trends, not the maximum potential improvement.

VIII. Conclusion

Lumped and distributed compact models for NC-FinFETs have been presented in this work. The models capture the characteristics that make NC-FET a candidate for future low power transistor due the possibility of achieving less than 60mV/dec and higher on-current. Floating metal gate case is modeled via lumped compact model, while distributed compact model is used for devices without floating metal. Clear $I-V$ and g_m differences between lumped and distributed devices are present in the strong inversion condition. The proposed models are implemented and tested in circuit simulators.

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