

# A Parameterized SPICE Macromodel of Resistive Random Access Memory and Circuit Demonstration

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## ABSTRACT

A parameterized SPICE macromodel of resistive random access memory (RRAM) is demonstrated to simulate the memory chip. The two-terminal RRAM model has the features of (1) initial condition settings of high resistance state (HRS) or low resistance state (LRS) (2) a forming behavior option (3) DC/transient mode selection (4) unipolar/bipolar mode selection, and (5) multilevel cell (MLC) operation. The features have been verified in the simulation of memory peripheral circuits with good convergence.

## I. INTRODUCTION

Nonvolatile memory (NVM) of the resistive switching family has been studied a lot these days as the next-generation memory beyond the mainstream flash memory. One of the most promising candidates is RRAM. Our previous work [1] has demonstrated an  $\text{HfO}_2$ -based bipolar RRAM with high yield and good reliability. Following that, this work presents a parameterized SPICE macromodel to facilitate the RRAM chip design. The SPICE model is based on the data extracted from the  $\text{HfO}_2$ -based RRAM. Fig. 1 shows the sandwich structure of the RRAM with top and bottom TiN electrodes. The Ti layer in the stack serves as an oxygen getter. It will produce more oxygen vacancies in the  $\text{HfO}_x$  layer for better resistive switching phenomenon [1].

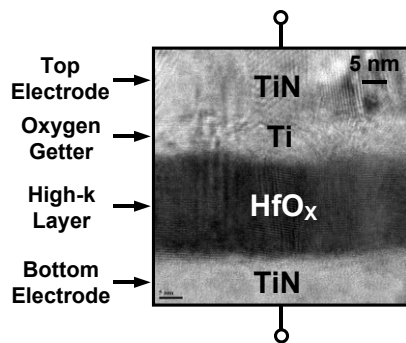


Fig. 1. TEM image of the structure of the  $\text{HfO}_2$ -based RRAM.

Before the memory chip goes into mass production, full chip SPICE modeling is indispensable to ensure correct functionality of the chip. Unlike MOSFET-based flash memory, SPICE modeling of RRAM needs to be engineered from scratch. In general, there are two ways of making SPICE models. The first one is called compact modeling, which is made by writing computer codes based on mathematical equations derived from device physics. A well-known example is the BSIM model for CMOS, which is written in C language. Note that we cannot do circuit simulation directly from these compact models. The codes need to be compiled and integrated into SPICE simulators to finish the task. The second one is called subcircuit method, which groups basic circuit components to represent a complex device. The subcircuit may or may not have physical meanings.

The inductor model and RFCMOS substrate network are two examples. Because this method does not need code compilation, it can be used with any SPICE simulator. Thus, though compact modeling is more flexible to design, we adopt the subcircuit method to make SPICE model for RRAM.

## II. RRAM CHARACTERISTICS

Fig. 2 shows a typical current-voltage ( $I$ - $V$ ) curve of the bipolar RRAM from measurement. For bipolar RRAM, opposite voltage polarity is needed to SET (to become LRS) and RESET (to become HRS) the device. In our sample,  $V_{\text{SET}}$  is positive and  $V_{\text{RESET}}$  is negative. The RRAM is in series with a transistor to form a 1T1R memory cell. The current compliance (CC) is set by the transistor gate voltage to prevent RRAM from dielectric breakdown. The heart-shaped  $I$ - $V$  trajectory is produced by sweeping the applied voltage from 0V to 1.5V, then backward to -1.4V, and finally to 0V. If we read the RRAM by applying a small voltage, say, 0.3V, the measured current ratio is larger than 100. This difference is large enough to represent logic 1 and 0 for the memory. Note that usually a process called forming is needed before RRAM starts resistive switching. During forming, a much larger positive voltage is applied to break RRAM down softly, which sets it to LRS.

The complete physical mechanism behind the resistive switching phenomenon is still under debate [3]-[7]. The physical mechanism varies with the types of the metal oxide and electrodes [7]. Among them, the theory of filament formation and rupture is the widely accepted one. The forming process creates the conducting filaments, which is the reason for LRS. The RESET process is explained by the rupture of filaments due to negative voltage-induced field. The SET process is explained by the formation of the previously ruptured filaments. This time LRS is reached at a smaller positive voltage  $V_{\text{SET}}$  than the forming voltage.

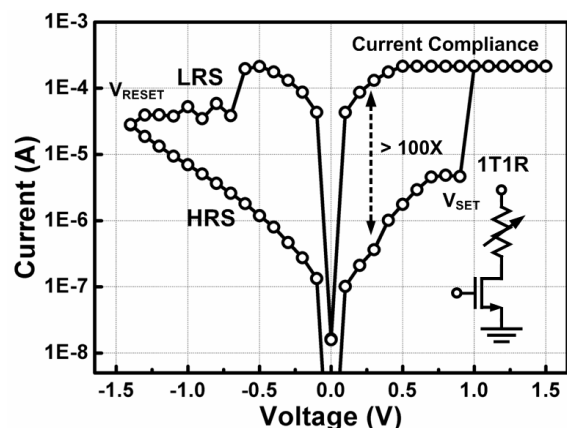


Fig. 2. Typical measured  $I$ - $V$  curve of the bipolar RRAM.

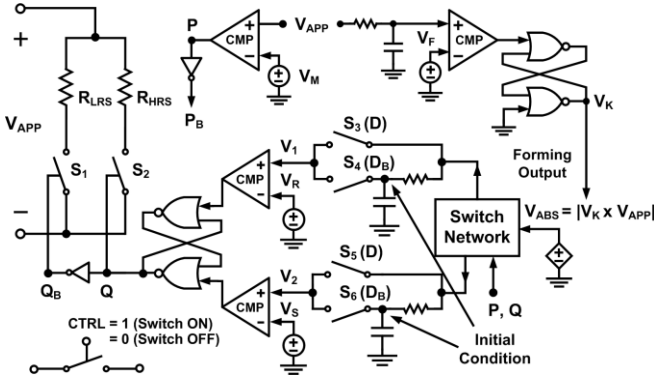


Fig. 3. SPICE macromodel for binary RRAM.

### III. SPICE MACROMODELS

Macromodels describe the device characteristics with an input-output relationship. Fig. 3 shows the schematic of the macromodel for binary RRAM. This model is written in HSPICE as a two-terminal subcircuit. The underlying idea is simple. The  $R_{LRS}$  and  $R_{HRS}$  are selected across the terminals by a decision procedure to represent resistive switching. However, the design challenge lies in the control technique of the decision procedure. How to control the timing to switch? How to make it switch according to the observed physics? This work provides a solution to these questions. Additionally, parameterization of the model creates a user-friendly interface for the circuit designers. For a real device, the forming process and RRAM access time need to be considered. This work includes these features to enhance the SPICE model.

In the following subsections, SPICE parameters in the model will be listed and explained first. Then we will discuss how the model works for binary and MLC operation. Finally, we briefly mention the switching mechanism of the RRAM.

#### A. SPICE Parameters

List of Parameters		
NAME	PARAM. = 1	PARAM. = 0
INI	HRS	LRS
FOR	Forming	No Forming
DCM	DC Mode (D = 1)	Transient Mode (D = 0)
UNI	Unipolar Mode ( $V_M = V_S$ )	Bipolar Mode ( $V_M = 0$ )
User-Definable: <b>VS:</b> SET Voltage <b>VF:</b> Forming Voltage <b>VR:</b> RESET Voltage (VF is activated when FOR = 1)		

Fig. 4. List of SPICE parameters in the model.

Fig. 4 is a summary table listing all SPICE parameters in the model. The parameter **INI** determines the initial resistance state of the RRAM. It is important for the circuit to know the initial resistance of the RRAM for DC convergence. The SPICE simulator cannot run smoothly in a transient simulation until DC convergence is reached. The parameter **FOR** indicates whether the forming feature is added. If **FOR** = 1, then parameter **VF** is enabled for the forming voltage. The parameters **DCM** and **UNI** are mode selectors. The parameter **DCM** indicates whether DC or transient analysis is performed. The parameter **UNI** indicates whether the RRAM is unipolar or bi-

polar as discussed in section II. In our case, the RRAM is bipolar and the transient analysis is performed. The SET and RESET voltage **VS** and **VR** are also user-definable parameters.

#### B. Binary Cell Operation

In Fig. 3, using building blocks such as logic gates, comparators, and switches lessens model complexity and enhances simulation speed. The switches are realized by voltage-controlled resistors. The control signal CTRL determines whether the switch is on or off. For clarity, the switch network is shown separately in Fig. 5.

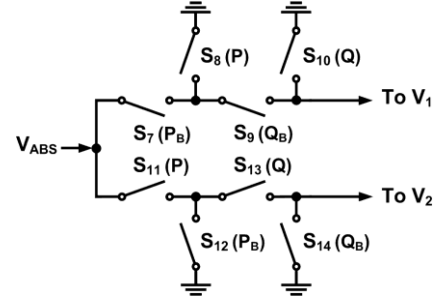


Fig. 5. Schematic of the switch network.

The circuit architecture is a self-consistent feedback system. First, the  $R_{HRS}$  and  $R_{LRS}$  are selected by the signal Q, which is latched by the cross-coupled NOR gates. The signal P is produced by comparing the applied voltage  $V_{APP}$  with  $V_M$ , which value is set by the parameter **UNI**. The signals P, Q and their complements are control signals of the switch network, which directs  $V_{APP}$  either to  $V_1$  or  $V_2$ . The  $V_{APP}$  are compared with the RESET voltage  $V_R$  or SET voltage  $V_S$  to determine the RRAM state. Note that there is a RC network inserted between  $V_1$  or  $V_2$  and the switch network. The RC time constants represent the switching time of the RRAM, which can be measured experimentally. The initial voltages at the capacitor nodes can be set via the parameter **INI**. In this way, there will be no DC convergence problem when the initial resistance of RRAM is determined. Because the capacitor is open in a DC simulation, another path must be formed to keep the feedback loop. This task is done by the switches  $S_3$  to  $S_6$ , which are controlled by the parameter **DCM**. Finally, if the forming option is activated via the parameter **FOR**,  $V_{APP}$  is compared with the forming voltage  $V_F$ . The resulting signal is sent to the cross-coupled NOR gates. Initially,  $V_K = 0$ . This corresponds to the RRAM in HRS until  $V_{APP}$  reach  $V_F$ , which makes  $V_K = 1$  for normal switching. Note that one input of the cross-coupled NOR gates is terminated to ground to ensure that the signal  $V_K$  will only be modified once.

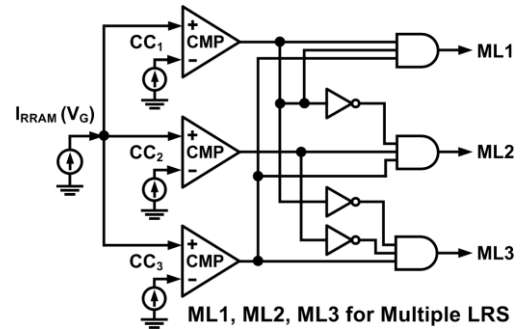


Fig. 6. Add-on circuit to realize three LRS levels.

### C. Multilevel Cell Operation

Two methods to realize MLC operation are described in [1]. The first is by adjusting the CC level to create multiple LRS. The second is by controlling the negative RESET voltage to create multiple HRS. Because the former method is more reproducible and suitable for memory array, we discuss the multiple LRS case here. In our flexible model architecture, we only need some add-on circuits to simulate MLC. Fig. 6 is an example of the add-on circuit to realize three-level LRS. The cell current is compared with three CC levels to produce digital signals ML1, ML2, and ML3 for three  $R_{LRS}$ . The  $I$ - $V$  simulation (lines) in Fig. 7 shows good agreement with measured data (points) for three LRS levels.

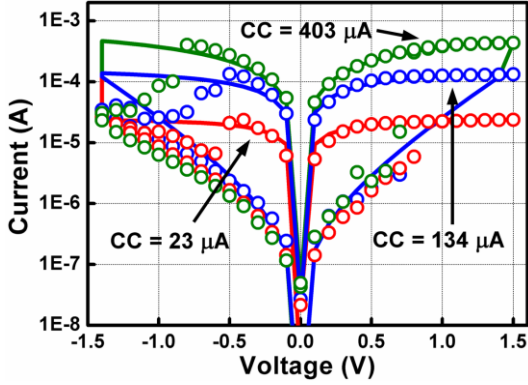


Fig. 7.  $I$ - $V$  simulation vs. measured data for three LRS levels.

### D. Switching Mechanism

From measurement we know the resistance values of HRS and LRS are a function of the applied voltage  $V_{APP}$ . Though a thorough physical explanation of HRS and LRS is not the purpose of this work, it is worth mentioning the mathematical equations used in the model. In Fig. 8, A two-segment space charge limited current (SCLC) model is used to describe LRS. Because of the limits of CC, the LRS in most operation shows only the linear region of the SCLC model.

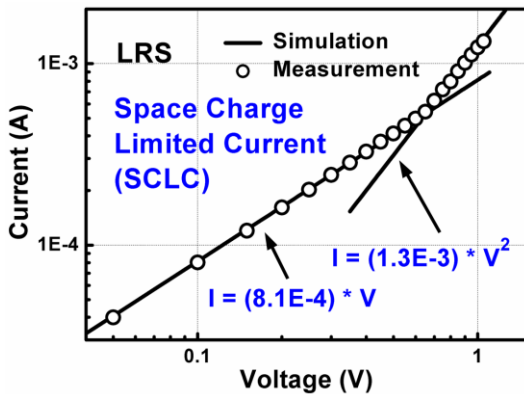


Fig. 8. A two-segment SCLC model for LRS.

On the other hand, a Schottky emission-like model is used to describe HRS. Fig. 9 shows the HRS current is exponentially dependent on the voltage. Both Fig. 8 and Fig. 9 are measured at room temperature. The mathematical equations and the fitting constants used in the model are shown in the figures.

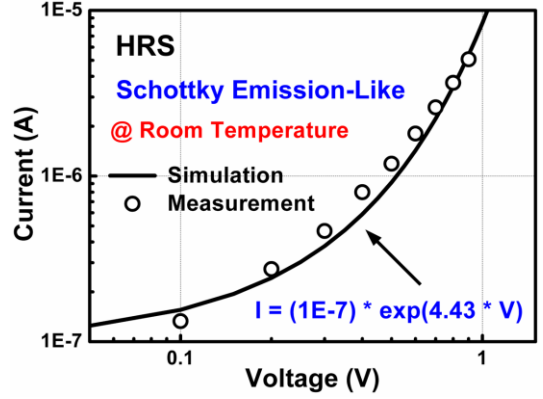


Fig. 9. Schottky emission-like model for HRS.

## IV. MODEL VERIFICATION

This section verifies the usability of the SPICE model in terms of functionality test and circuit demonstration.

### A. Functionality Test of 1T1R Cell

Fig. 10 tests the initial resistance setting with  $INI = 0$  and  $INI = 1$ . The READ, SET (Write “0”), and RESET (Write “1”) voltages are 0.2V, 1.5V, and -1.4V, respectively. The programming pulse width is 15ns. The resistance states after READ are correct for both initial conditions. Note that at this stage, the SET, RESET, and READ processes are carried out directly on 1T1R cell without memory peripheral circuits.

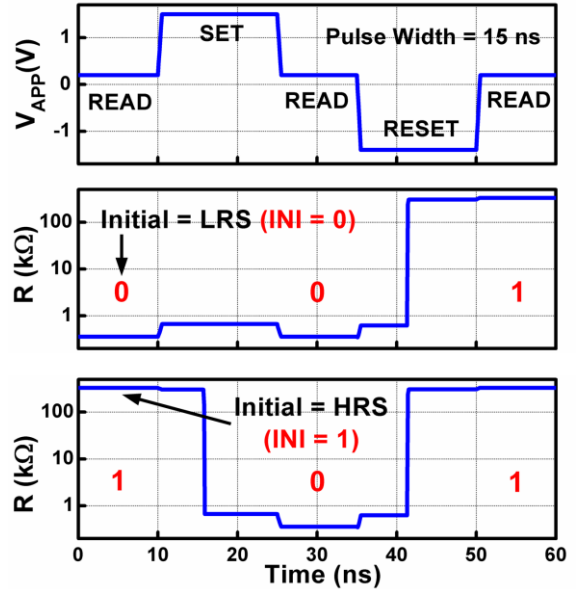


Fig. 10. Test of initial resistance setting of the 1T1R cell.

Fig. 11 tests the forming behavior with  $V_F = 4V$  and  $V_F = 1V$ . The  $V_{APP}$  waveform is the same as in Fig. 10. For  $V_F = 4V$ , the RRAM state maintains in HRS because  $V_{APP} < V_F$ . For  $V_F = 1V$ , RRAM switch to LRS after a specific switching time after  $V_{APP}$  reaches 1V.

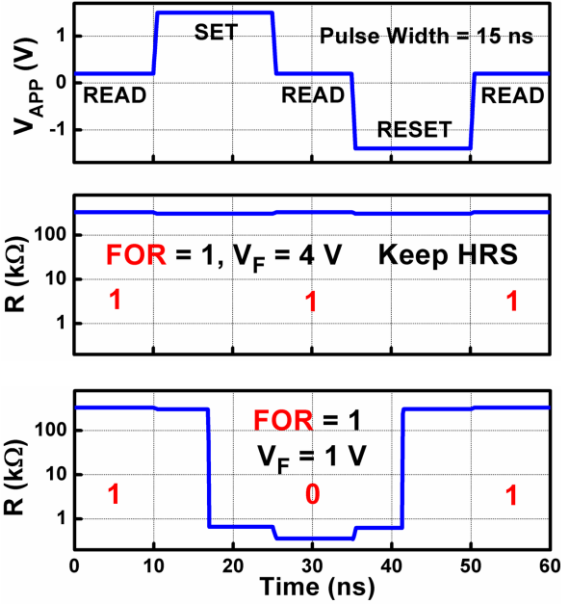


Fig. 11. Test of the forming behavior of the 1T1R cell.

### B. Circuit Demonstration

After the functionality test, the 1T1R cell is integrated with the memory peripheral circuits to do full SPICE simulation. In Fig. 12, we integrate four RRAM cells with the READ circuit architecture implemented in [2]. The bit lines (BL) along with the parasitic capacitance  $C_p$  are selected by signals BL\_SEL of the transmission gates. The READ driver then sends analog signals BL\_OUT to the sense amplifier (SA) for digital signals SA\_OUT. Fig. 13 shows the test results of the READ process. We first specify the bit information in the four cells via **INI** = 0, 1, 0, 1. Then we apply signals BL\_SEL to consecutively select from BL1 to BL4 with  $V_{dd} = 3.3$  V. Finally, the stored bits can be read from SA\_OUT correctly with  $V_{dd} = 1.8$  V.

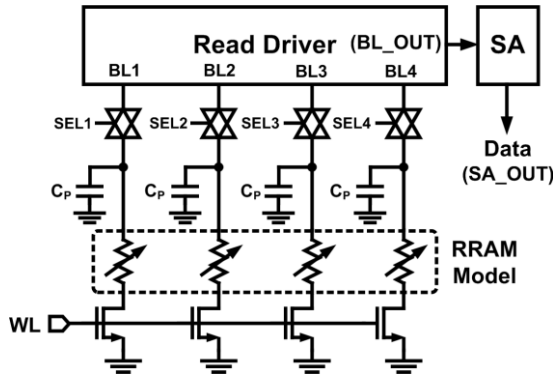


Fig. 12. Architecture of the READ circuit with four RRAM cells.

Fig. 14 shows the layout of the RRAM array with READ, WRITE circuits, control (CTRL) logic, and multiplexer (MUX) circuits.

## V. CONCLUSION

SPICE model plays a bridging role between device fabrication and circuit implementation in any mature technology. In this work, we have demonstrated the making of a parameterized SPICE model for RRAM using subcircuit method. For future scaling of the RRAM,

it is critical to understand the physics behind the switching phenomenon and put it into the SPICE model.

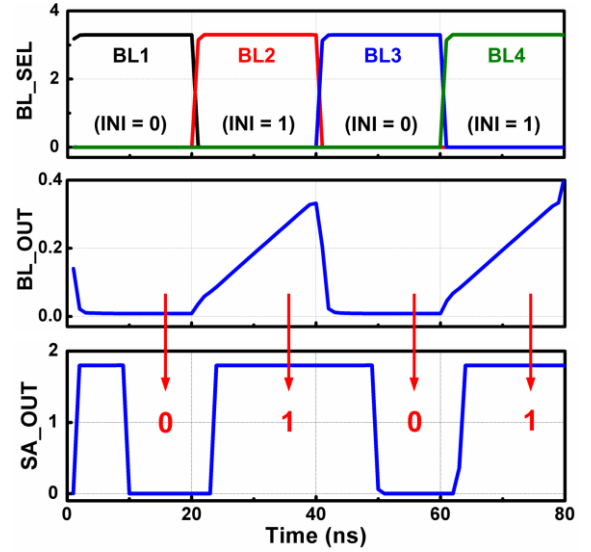


Fig. 13. Simulation results of the READ architecture with four RRAM cells.

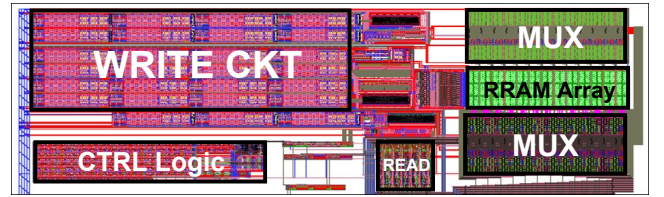


Fig. 14. Layout of the designed RRAM chip.

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