Modeling of Subsurface Leakage Current in Low V_{TH} Short Channel MOSFET at Accumulation Bias

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***Abstract*— We present a phenomenological model for subsurface leakage current in MOSFETs biased in accumulation. The subsurface leakage current is mainly caused by source–drain coupling, leading to carriers surmounting the barrier between the source and the drain. The developed model successfully takes drain-to-source voltage (V_{DS}), gate-to-source voltage (V_{GS}), gate length (L_G), substrate doping concentration (N_{sub}), and temperature (T) dependence into account. The presented analytical model is implemented into the BSIM6 bulk MOSFET model and is in good agreement with technology-CAD simulation data.**

***Index Terms*— BSIM6, leakage, modeling, short channel, subsurface, zero-V_{TH} MOSFET.**

I. Introduction

THERE are various types of leakage currents, such as gate-induced drain leakage (GIDL) current, drain-to-body/source-to-body junction leakage currents [1], and gate leakage current [2], in OFF-state planar MOSFETs. GIDL is modeled by using band-to-band tunneling model [3], and it can be reduced by introducing lightly doped drain (LDD) structure to lower the electric field [4]. All leakage currents in the MOSFETs have been successfully modeled and are available in the BSIM6 MOSFET model [5]. However, it is important to consider the leakage path between the source and the drain beneath the channel, which has not received much attention in the literature [6]–[8]. Zhu *et al.* [9] have analyzed the punchthrough currents and corresponding potential distribution for long-channel MOSFET at high drain voltage but lacked a suitable model for circuit simulation. Although the heavily doped substrate and the employment of the halo doping could suppress the punchthrough effect, they may result in significant band-to-band tunneling current through drain/source–body junctions [10]. Furthermore, even though there is a parasitic bipolar-junction transistor (BJT) comprising source–body–drain (emitter–base–collector) in the MOSFET [11], it is generally impossible to attribute the OFF-state leakage current to BJT current, because body–source (base–emitter) junction is not forward biased. In addition to the MOSFETs, the leakage current underneath the fin (channel) at OFF-state is also observed in FinFETs [12]. Thus, it is crucial to have an insight into the physics of leakage current via the path beneath the channel and the corresponding model. In this paper, we propose a model to describe the subsurface leakage current by taking drain-to-source voltage (V_{DS}), gate-to-source voltage (V_{GS}), gate length (L_G), substrate doping concentration (N_{sub}), and temperature (T) into account for the short-channel MOSFET. The root cause of the subsurface leakage current is that the barrier height between the source and the drain is lowered mainly by V_{DS}, giving rise to electrons transport across that barrier. The developed model built into the BSIM6 exhibits good match with technology computer-aided design (TCAD) simulation data.

This paper is organized as follows. In Section II, we discuss in detail about the physics of the subsurface leakage current including the key factors that affect it, and present an analytical model. In Section III, we present and discuss the results of our model incorporated in the BSIM6 model by comparing it with TCAD simulations. We conclude this paper in Section IV.

II. Model Description

The nMOSFET structure simulated in Sentaurus TCAD [13] with gate oxide thickness $T_{ox} = 2$ nm, $N_{sub} = 10^{17}$ cm^{-3}, is shown in Fig. 1(a). The peak value of Gaussian doping profile of source (drain) is 10^{20} cm^{-3}, while that of source (drain) extension is 10^{19} cm^{-3} in order to minimize the GIDL effect [4]. The physical models used in simulations include doping-dependent mobility with high-field saturation and degradation, van Dort quantization, Shockley–Read–Hall, and Schenk band-to-band tunneling models [13]. Note that we choose the zero-threshold-voltage devices because they have low doping [14], and the subsurface leakage phenomenon is highly visible in these devices, which will be discussed in Section II-C. The zero threshold voltage devices can be

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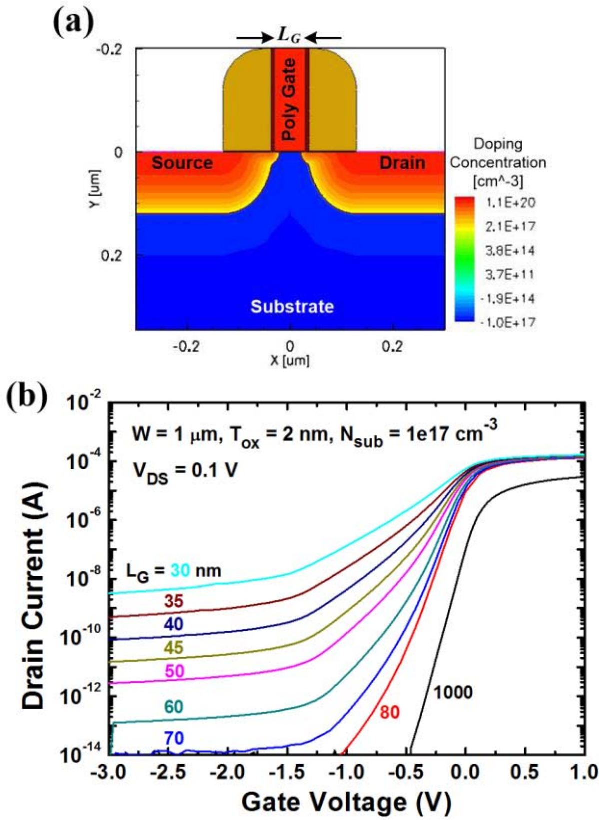

Fig. 1. (a) Simulated structure of nMOSFET with doping concentration. (b) Simulated I_{DS}–V_{GS} curves for different values of L_G at $V_{DS} = 0.1$ V and $V_S = V_B = 0$ V. It shows that the subsurface leakage current at the accumulation bias region increases as the value of L_G reduces.

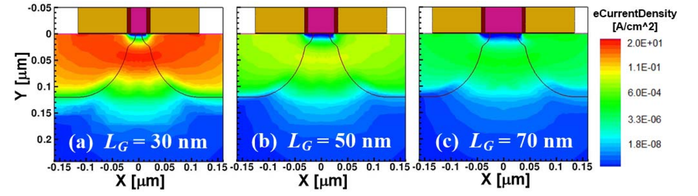

Fig. 2. Contour plots of the electron current density for nMOSFET with the gate length of (a) 30, (b) 50, and (c) 70 nm at $V_{GS} = -3$ V, $V_{DS} = 0.1$ V, and $V_S = V_B = 0$ V. The junction depths of source/drain and their extensions are 120 and 20 nm, respectively.

used in electrostatic discharge and I/O as well as some analog/RF applications [14], [15]. Fig. 1(b) shows the simulated drain current versus gate-to-source voltage characterization for nMOSFETs for different gate lengths at $V_{DS} = 0.1$ V. It can be observed that there is an approximately gate bias-independent (in a log scale) leakage current in the strong accumulation bias region and depends on the gate length. This leakage current cannot be explained by GIDL, p-n (drain-to-body) junction leakage, or parasitic BJT current. The GIDL current should increase as the gate bias becomes more negative and it can be effectively suppressed by LDD structure [4]. Furthermore, the p-n (drain-to-body) junction leakage in reverse bias is generally independent of the gate length [1]. Parasitic BJT current cannot also be considered in this case because source–body junction is not forward biased. Therefore, a new model should be developed to capture this leakage current by taking the key device parameters into account.

A. Drain-to-Source Voltage and Gate Length Dependence

Fig. 2(a)–(c) shows the contour plots of electron currents for the devices with the gate length of 30, 50, and 70 nm at $V_{GS} = -3$ V and $V_{DS} = 0.1$ V, respectively. It can be observed that there are electron current paths at a distance away from the Si/SiO_2 interface which we define as subsurface leakage current. Moreover, the subsurface leakage current is gate length-dependent, as shown in Fig. 1(b). This can be directly attributed to the barrier lowering induced by V_{DS}, which is similar to drain-induced barrier lowering effect [16] but at the different depths. For a shorter channel device, even a small V_{DS} can sufficiently reduce the barrier height between the source and the drain, so that the electrons are able to surmount the barrier from the source side and the corresponding current will be similar to the diode current form. Fig. 3(a) shows the conduction band diagram and the extracted barrier height lowering (see the data in black in the inset) at the local minimum of conduction band due to V_{DS} of the device with $L_G = 50$ nm from the TCAD simulations. We approximate the barrier change as a linear function for simplification

$$\Delta V = A \cdot V_{DS} \quad (1)$$

where A (dimensionless) is a fitting parameter defined as barrier-change coefficient that is obtained from the TCAD data. We consider the gate length-dependence of the subsurface leakage current to be exponential relationship from the observation in Fig. 3(b), which shows that the slopes in a log scale for different V_{DS} values are approximately the same. In addition, Fig. 3(c) shows that the drain current exponentially depends on V_{DS}, although the curves are slightly deviating from exponential behavior at high V_{DS} due to nonlinear barrier height lowering shown in the inset of Fig. 3(a) (black). The root cause of this nonlinear effect comes from the space-charge effect influenced by the high injection current, because the injected electrons can screen out the electric field provided by the drain terminal and hence decrease barrier height lowering [17]. The data in red in the inset of Fig. 3(a) fortify the above hypothesis. If the mobility is low enough to reduce the drift current across the drain–body reverse-biased junction, the barrier height lowering will be much more linear, implying that the injected electrons actually are able to affect the electrostatics. Nevertheless, the linear approximation is still adopted for simplification. Thus, the subsurface leakage current can be expressed as

$$I_{DS,\text{leakage}} = C \cdot e^{-B \cdot L_G} \cdot \left(e^{\frac{A \cdot V_{DS}}{V_t}} - 1\right) \cdot W \quad (2)$$

where W is the device width in units of m, V_t is the thermal voltage ($=kT/q$), and B and C in units of m^{-1} and A/m are the variables called inverse characteristic length and intrinsic leakage that will be discussed in Section II-C. It should be noted that (2) guarantees that the leakage current must be zero when $V_{DS} = 0$. Furthermore, if L_G is long enough

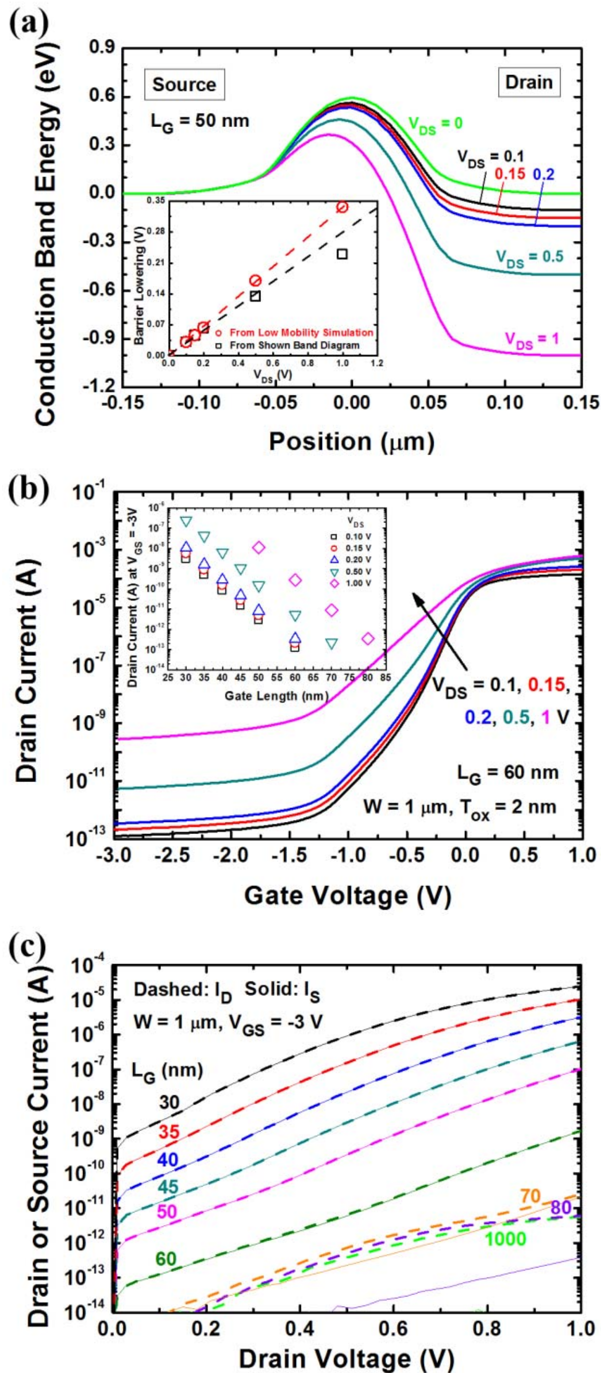

Fig. 3. (a) Conduction band diagram of device with $L_G = 50$ nm at different values of V_{DS} but at fixed $V_{\mathrm{GS}} = -3$ V and $V_{\mathrm{S}} = V_{\mathrm{B}} = 0$ V at a depth of 50 nm away from $\mathrm{Si/SiO_2}$ interface where there is a local minimum of barrier height along the vertical direction. Inset: barrier lowering extracted from the band diagram (black) and from low-mobility simulation for low space-charge effect (red). (b) I_{DS}–V_{GS} curves of device with $L_G = 60$ nm for different values of V_{DS}. Inset: drain current at $V_{\mathrm{GS}} = -3$ V versus gate length for different values of V_{DS}. (c) Drain and source currents versus drain voltage curves for different values of L_G.

[for example, $L_G > 70$ nm, as shown in Fig. 3(c)] to decouple the source and the drain, the source current is much smaller than the drain current and, the drain current is almost independent of L_G, meaning that the reverse-biased junction leakage dominates the drain current, as shown in Fig. 3(c).

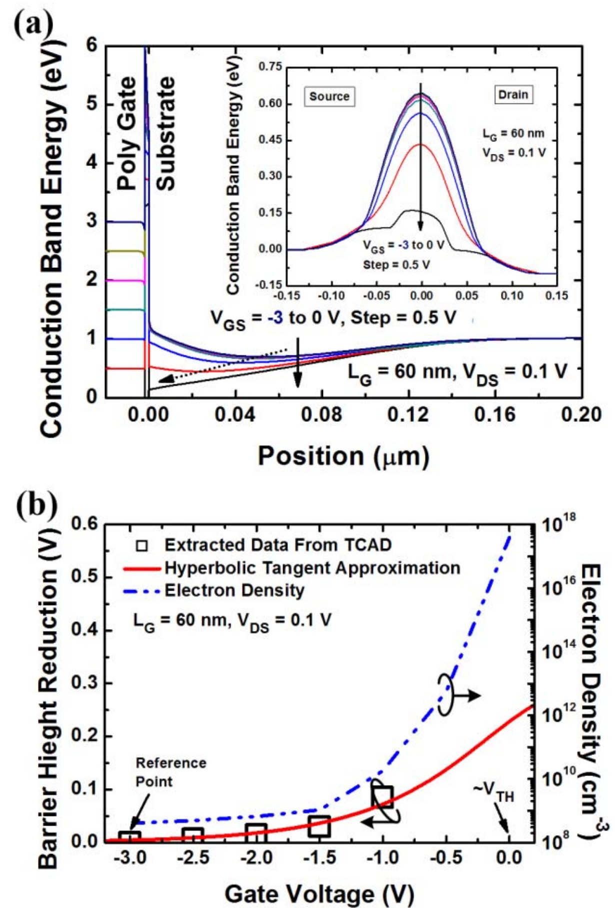

Fig. 4. (a) Conduction band diagram in the vertical direction (from gate to substrate) and the lateral direction (from source to drain) (inset). (b) Barrier height reduction for different gate voltages extracted from (a). Hyperbolic tangent function approximation (red) is used in the model. As V_{GS} is close to V_{TH}, the electron density near the surface grows up dramatically, meaning that the barrier height reduction (band bending) leads to normal transistor current.

B. Impact of Gate-to-Source Voltage

As the gate voltage sweeps from the strong accumulation bias to around the flat-band voltage (V_{FB}), the local minimum of conduction band decreases further and moves toward the $\mathrm{Si/SiO_2}$ interface [see Fig. 4(a) (dashed arrow)], which means that the leakage current is gate voltage-dependent at the transition region from accumulation to weak inversion. Before the accumulation layer is completely formed, the gate field can penetrate into the substrate, leading to V_{GS}-dependent barrier height reduction. If the accumulation layer is built, the gate electric field will be screened out by the accumulated holes, resulting in V_{GS}-independent behavior. Nevertheless, the V_{GS}-dependent effect will no longer be prominent when V_{GS} is close to or higher than the threshold voltage (V_{TH}). In other words, if the channel is inverted, the subsurface leakage would mix with the normal transistor current and is negligible. Fig. 4(b) shows that the barrier height reduction due to V_{GS} increases exponentially for more positive V_{GS} with respect to $V_{\mathrm{GS}} = -3$ volt. However, the presence of the normal transistor current is not considered in the extraction of the barrier height reduction in Fig. 4(b). The reduction

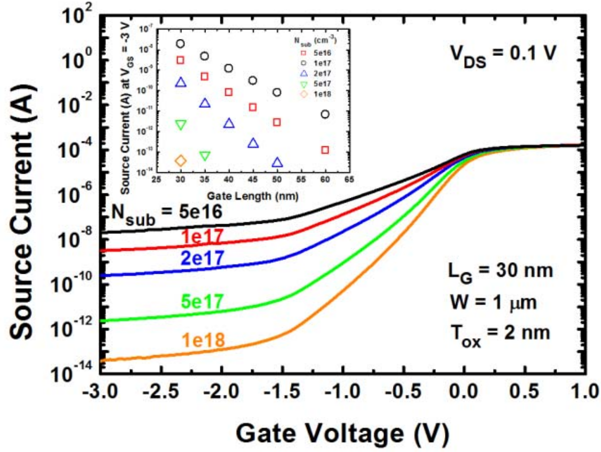

Fig. 5. I_{DS}–V_{GS} curves for nMOSFET with $L_G = 30$ nm at $V_{DS} = 0.1$ V and $V_S = V_B = 0$ V for different N_{sub} values. Inset: I_{DS} at $V_{GS} = -3$ V and $V_{DS} = 0.1$ V for different values of L_G and N_{sub}.

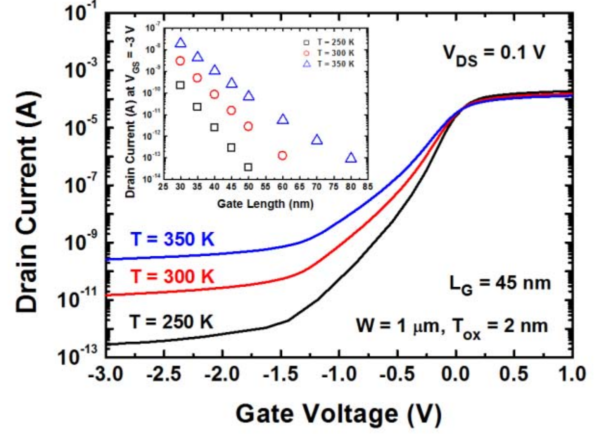

Fig. 6. I_{DS}–V_{GS} curves for nMOSFET with $L_G = 45$ nm at $V_{DS} = 0.1$ V and $V_S = V_B = 0$ V for different T values. Inset: I_{DS} at $V_{GS} = -3$ V and $V_{DS} = 0.1$ V for different values of L_G and T.

should gradually saturate when V_{GS} is close to or higher than V_{TH}, where the band bending is for the formation of electron inversion layer. We model V_{GS} effect on barrier height change as an exponential function inside the hyperbolic tangent function

$$\Delta\phi = D \cdot \tanh(\exp(E \cdot (V_{GS} - V_{TH}))) \tag{3}$$

where D and E in units of V and V^{-1} are the V_{GS}-associated fitting parameters that can be determined from the TCAD data, as shown in Fig. 4(b). The threshold voltage (V_{TH}) will be automatically calculated by BSIM6 model [18]. Therefore, from (2), the subsurface leakage current can be rewritten as

$$I_{DS,leakage} = C \cdot e^{-B \cdot L_G} \cdot e^{\frac{\Delta\phi}{V_t}} \cdot \left(e^{\frac{A \cdot V_{DS}}{V_t}} - 1\right) \cdot W. \tag{4}$$

C. Substrate Doping and Temperature Dependence

In the TCAD simulation results of Fig. 1(b), the uniform substrate doping N_{sub} is adopted for simplification. It is evident that in Fig. 5, the subsurface leakage current is inversely proportional to N_{sub}, because a heavily doped substrate can reduce the depletion width of source- and drain-to-body and, hence, coupling. However, if N_{sub} is high enough (for example, 10^{18} cm^{-3}), the GIDL current can overwhelm the subsurface leakage current in the drain current due to high electric field [10], [16]. Thus, we only plot the source currents in Fig. 5 in order to get rid of the GIDL currents and make the subsurface leakage current clear. If N_{sub} is not fairly high, based on Fig. 5 (inset), the leakage currents at $V_{GS} = -3$ V are still linear but with different slopes in a log scale for different N_{sub} values, which implies that the doping effect can be simply modeled by letting the variables B and C be doping concentration-dependent with respect to 10^{23} (m^{-3})

$$B = B_0 \left(\frac{N_{sub}}{10^{23}}\right)^{\text{EXP1}}$$

$$C = C_0 \exp\left(-\left(\frac{N_{sub}}{10^{23}}\right)^{\text{EXP1}}\right)$$

where N_{sub} is in units of m^{-3}, and B_0, C_0, and EXP1 are the fitting parameters. If the doping concentration between the source and the drain is high enough to avoid coupling of the drain-to-body and source-to-body junction depletion regions, the subsurface leakage current can be blocked by the barrier. A complicated doping profile can also suppress the leakage. For example, carrying out the halo implantation and adopting the retrograde doping can suppress the leakage current. It is worth noting that although the substrate doping profile in a real device is sophisticated so that the V_{DS} dependence is not significant, as shown in Fig. 3(b), the barrier-change coefficient A can be set to a small value for matching the experimental data.

In addition to N_{sub}, the temperature dependence should also be included in the model. Due to more energetic electrons at higher temperature passing the barrier, the subsurface leakage would increase as the temperature rises, as shown in Fig. 6. Fig. 6 (inset) shows the leakage current versus gate length curves for different temperatures, and it can be observed that they are linear functions but with different slopes in a log scale for different temperatures just like N_{sub} effect, so a fitting parameter EXP2 is introduced to capture the temperature effect. As a result, variables B and C can finally be expressed as

$$B = B_0 \left(\frac{N_{sub}}{10^{23}}\right)^{\text{EXP1}} \left(\frac{300}{T}\right)^{\text{EXP2}} \tag{5}$$

$$C = C_0 \exp\left(-\left(\frac{N_{sub}}{10^{23}}\right)^{\text{EXP1}} \left(\frac{300}{T}\right)^{\text{EXP2}}\right) \tag{6}$$

where T is in units of K. From (4), the complete form of subsurface leakage current is

$$I_{DS,leakage} = C(N_{sub}, T) \cdot e^{-B(N_{sub},T) \cdot L_G} \cdot e^{\frac{\Delta\phi}{V_t}} \cdot \left(e^{\frac{A \cdot V_{DS}}{V_t}} - 1\right) \cdot W. \tag{7}$$

III. Results and Discussion

The model of subsurface leakage current (7) and related parameters is incorporated in the BSIM6 model [5].

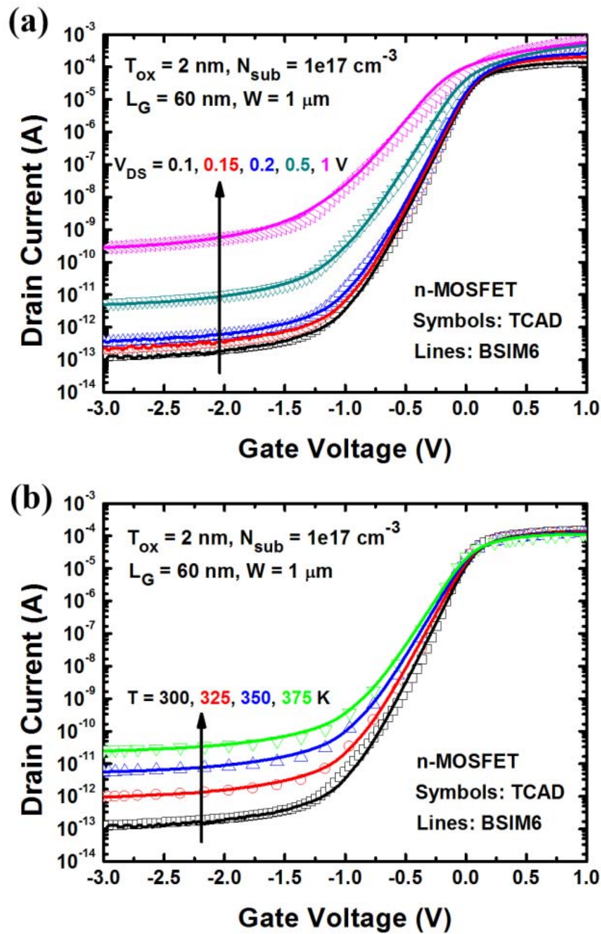

Fig. 7. Comparison of TCAD and BSIM6 with (7) for nMOSFET with $L_G = 60$ nm at $V_S = V_B = 0$ V for (a) different values of V_{DS} and (b) different temperatures.

Fig. 7(a) and (b) shows the comparison of the TCAD simulation data with the SPICE simulation results for different V_{DS} values (from linear to saturation bias regimes) and temperatures for an nMOSFET with the gate length of 60 nm, the device width of 1 μm, the substrate doping of 10^{17} cm^{-3}, and the gate oxide thickness of 2 nm, respectively. Fig. 7(a) and (b) are with the same set of fitting parameters. The developed model exhibits good match with the TCAD simulation data. The V_{GS} effect appears at around flat-band voltage V_{FB} (~ -1 V) and is successfully included in model. Equation (7) captures not only the barrier lowering due to V_{DS} but also the current increment caused by rising temperature. It is worth noting that the influence of the junction depths X_j of source and drain is not explicitly modeled in this paper. As X_j is shallower, the leakage path is much closer to the surface and the leakage is suppressed because of better gate control, as shown in Fig. 8(b). The junction depth effect can be included by adjusting the intrinsic leakage C and barrier-change coefficient A. Nevertheless, a shallow junction could result in higher series resistance and thus degrade the device performance [19]. In addition to X_j, the gate oxide thickness would also affect the subsurface leakage current. If the gate oxide is thicker (less gate control), the subsurface

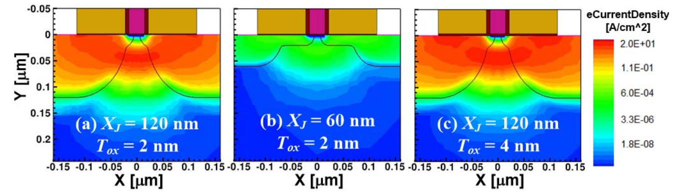

Fig. 8. Contour plots of the electron current density for $L_G = 30$ nm nMOSFET with (a) $X_j = 120$ nm and $T_{ox} = 2$ nm (for reference), (b) $X_j = 60$ nm and $T_{ox} = 2$ nm, and (c) $X_j = 120$ nm and $T_{ox} = 4$ nm at $V_{GS} = -3$ V, $V_{DS} = 0.1$ V, and $V_S = V_B = 0$ V.

leakage current would be prominent, because drain/source–body capacitance overcomes the gate capacitance, as shown in Fig. 8(c), even though the halo doping or the retrograde doping is adopted (not shown). Similar to X_j, the gate oxide effect can be captured by adjusting C and A to suitable values.

IV. Conclusion

A subsurface leakage current model is developed phenomenologically based on the TCAD simulation. The subsurface leakage current is generally caused by the barrier height reduction between the source and the drain influenced by V_{DS} at a distance from the Si/SiO_2 interface. V_{GS} can also affect the barrier height but only significant near V_{FB}. As gate length is scaled down, the current increases due to stronger source to drain coupling. Furthermore, N_{usb} and T are the important factors. When N_{sub} becomes heavier, the depletion widths of junctions reduce and hence lower leakage current. As T rises, there are more electrons with enough energies to surmount the barrier, so that the leakage current increases further. The above effects are successfully included in the developed model. Finally, the model is implemented into the BSIM6 model and is in good agreement with the TCAD simulation for different V_{DS} values and temperatures.

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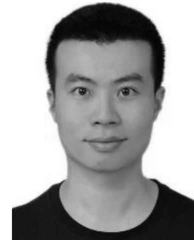

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