

A Predictive Tunnel FET Compact Model With Atomistic Simulation Validation

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Abstract—A predictive tunnel FET compact model is proposed. Gaussian quadrature method is used to overcome the challenge of integration. This provides the flexibility to use Wentzel–Kramers–Brillouin under spatially varying electric field, to incorporate effective band edge states broadening, and to evaluate the drain current by Landauer equation with consideration of electron reflection at the tunnel junction. The model not only shows good accuracy, speed, and smoothness, but is also some predictive capability so that the effects of changing material parameters on IC characteristics are well captured. The model is validated with atomistic simulation data for several materials.

Index Terms—Compact model, Gaussian quadrature, Landauer equation, tunnel FET (TFET).

I. INTRODUCTION

TUNNEL FET (TFET) is a promising candidate for low power applications [1], [2] due to its potential to be operated at very low V_{DD} due to its steep subthreshold slope and thus very low switching energy [3], [4]. In order to explore the TFET-based circuit, a robust compact model is required. Although compact models of TFETs are available in the literature [5]–[8], the electric field of the tunneling junction is always assumed to be constant over the energy range in the junction, resulting in inaccurate tunneling probability. To take nonuniform electric field into account, the tunneling current should be described by Landauer equation [9], which sums up all possible tunneling paths over the tunneling window. However, brute force integration of the Landauer equation for tunneling probability and carrier distribution is numerically inefficient [10], [11]. In this paper, to overcome this numerical challenge, we apply the Gaussian quadrature method [12], [13] for the first time to develop compact model of tunnel devices. This enables us to directly integrate Landauer equation with Wentzel–Kramers–Brillouin (WKB)-based tunneling, Fermi

distribution function, and band edge tailing, resulting in a more accurate and predictive compact model.

This paper is organized as follows. In Section II, we discuss in detail about the physics of TFETs and derivation of the analytical model. In Section III, the accuracy, speed, and smoothness of proposed model are analyzed. The comparisons of model and atomistic simulations for several materials and device structures are also presented. We conclude this paper in Section IV.

II. MODEL DESCRIPTION

The TFET in this model is treated as a tunnel diode in series with an MOSFET [5]. Because the tunneling current is much smaller than the drift-diffusion current in the MOSFET, the TFET current is generally limited and determined by the tunneling. Instead of using Kane's model with a constant electric field across the tunnel junction as in literature [5]–[8], the TFET band-to-band tunneling current at the tunnel junction in this paper is described by Landauer equation [9]

$$I = \frac{2q}{h} \int M(E)T(E) [f_S(E) - f_{CH}(E)] dE \quad (1)$$

where M is the dimensionless number of the conduction (tunneling) modes, T is the tunneling probability, and f_S and f_{CH} are the Fermi distribution functions of source and channel

$$f_S(E) = \frac{1}{1 + \exp[(E_{FS} - E)/kT]} \quad (2)$$

$$f_{CH}(E) = \frac{1}{1 + \exp[(E_{FS} + qV_{DS} - E)/kT]} \quad (3)$$

Fig. 1 shows the schematic of a multigate TFET and its band diagram in the ON-state. In order to calculate the tunneling probability, the potential profile of source–channel junction is required. The electrostatics can be solved from Poisson equation with boundary conditions set in Fig. 1 and continuous electric field at $x = 0$ [10], [14], [15], resulting in the following potential expression of each region:

$$\varphi_{S1}(x) = \frac{qN_S}{2\epsilon_S}(x + L_1)^2 \quad (4)$$

$$\varphi_{S2}(x) = (V_{GS} - V_{FBS}) - \frac{(V_{GS} - V_{FBB} - \varphi_{CH})}{2} \exp\left(\frac{x - L_2}{\lambda}\right) \quad (5)$$

where N_S is the source doping concentration, ϵ_S is the source permittivity, V_{FBS} and V_{FBB} ($= V_{FBS} + V_{bis}$) are the flat-band

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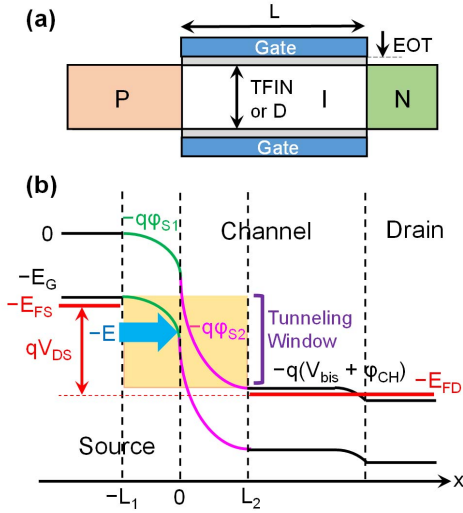


Fig. 1. (a) Multigate TFET. $TFIN$ is the fin thickness and D is the nanowire diameter. (b) Band diagram when device is on.

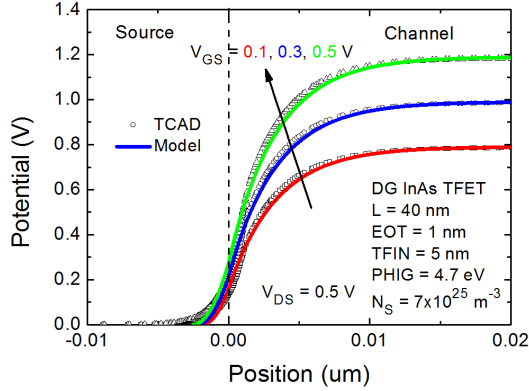


Fig. 2. Surface potential profiles at various biases in a DG InAs FET. The model results are in good agreement with TCAD simulations.

voltages of the source and channel, V_{bis} is the built-in potential of the source-channel junction, λ is the characteristic length determined by the device geometry [16], ϕ_{CH} is the surface potential in the channel, which is determined by both V_{GS} and V_{DS} [10], [17] using the BSIM CMG unified FinFET and nanowire-FET compact model [18], and L_1 and L_2 are the high-field region widths in the source and channel give by

$$L_1 = \sqrt{\frac{2\epsilon_S\phi_S(0)}{qN_S}} \quad (6)$$

$$L_2 = \lambda \ln \left[\frac{2 \cdot (V_{GS} - V_{FBS} - \phi_S(0))}{V_{GS} - V_{FBS} - V_{bis} - \phi_{CH}} \right] \quad (7)$$

where

$$\phi_S(0) = -\sqrt{(V_{GS} - V_{FBS} - \phi_{CH})^2 + 2(V_{GS} - V_{FBS})\Phi} + \Phi \quad (8)$$

$$\Phi = qN_S\lambda^2/\epsilon_S. \quad (9)$$

Fig. 2 shows the model results of the surface potential profiles at various V_{GS} in a 40-nm double-gate InAs TFET are in good agreement with 2-D TCAD simulations [19].

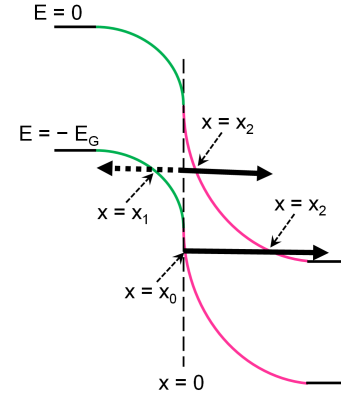


Fig. 3. Band diagram of the tunneling junction. The green and pink curves represent the bands of source and channel regions, respectively.

A. WKB-Based Tunneling Probability

The WKB approximation [20] is a useful method to evaluate the tunneling probability, even though there are some limitations like wave function mismatch at high electric field region [21], leading to overestimation of the tunneling probability, which will be addressed later by including the electron wave reflectance. Based on WKB approximation, the probability for a carrier to tunnel through a barrier with potential energy $V(x)$ can be expressed as

$$T(E) = \exp \left[-\frac{2\sqrt{2m^*}}{\hbar} \int \sqrt{V(x) - K} dx \right] \quad (10)$$

where m^* is the carrier effective mass, \hbar is the reduced Planck's constant, and K is the carrier energy. The potential energy of the tunneling junction can be divided into two regions: source [$V(x) = q\phi_{S1}(x)$] and channel [$V(x) = -q\phi_{S2}(x)$], as shown in Fig. 3. Consider the carrier with energy $-E$ ($E > 0$). In source region, the tunneling probability can be evaluated by using the boundary condition $q\phi_{S1}(x_1) - E + E_G = 0$, and the upper and lower limits are 0 and x_1 . The integration result is

$$A(E) = \frac{1}{2} \left[\frac{L_1 \sqrt{-\alpha + q\phi_S(0)} + \frac{\alpha \ln[\sqrt{\beta-\alpha}]}{\sqrt{\beta}}}{-\frac{\alpha \ln[\beta L_1 + \sqrt{\beta-\alpha+q\phi_S(0)}]}{\sqrt{\beta}}} \right] \quad (11)$$

where $\alpha = E - E_G$ and $\beta = q^2 N_S / (2\epsilon_S)$. Note that, α should be smoothed to be $q\phi_S(0)$ to ensure the $T(E)$ of source region at high E is unity, because at high E , the source barrier is infinitesimally thin. In the channel region, the boundary conditions are $q\phi_{S2}(x_2) + E = 0$ for low energy region (i.e., adjacent to source; the upper and lower limits are x_2 and 0) and $q\phi_{S2}(x_0) + E = E_G$ and $q\phi_{S2}(x_2) + E = 0$ for high energy region (i.e., only through channel; the upper and lower limits are x_2 and x_0). These boundary conditions give two results of the integral in (10)

$$B(E) = 2\lambda \left[\sqrt{E - q\phi_S(0)} - \sqrt{\gamma} \tan^{-1} \left(\frac{\sqrt{E - q\phi_S(0)}}{\sqrt{\gamma}} \right) \right] \quad (12)$$

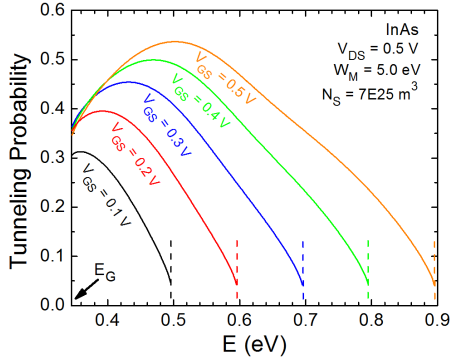


Fig. 4. Tunneling probability in an InAs TFET. Dashed lines: edges of tunneling windows.

and

$$B(E) = 2\lambda \left[\sqrt{E_G} - \sqrt{\gamma} \tan^{-1} \left(\frac{\sqrt{E_G}}{\sqrt{\gamma}} \right) \right] \quad (13)$$

where $\gamma = qV_{GS} - qV_{FBS} - E$. Equations (12) and (13) can be combined by smoothing $E - q\phi_S(0)$ to be E_G , when E is large. Therefore, from (11)–(13), the band-to-band tunneling probability can be expressed as

$$T(E) = \exp \left\{ -\frac{2\sqrt{2m^*}}{\hbar} [A(E) + B(E)] \right\}. \quad (14)$$

Fig. 4 shows the tunneling probability as a function of energy using InAs material parameters for different gate biases (V_{GS}), indicating that the tunneling window and probability increase with V_{GS} .

As mentioned earlier, the drawback of WKB approximation is the mismatch of the electron wave function at high electric field region [21], [22], leading to reflection at the boundary. To overcome this issue, a bias-independent electron wave reflectance R is introduced [21] so that (1) becomes

$$I = \frac{2q}{h} (1 - R) \times \int_{E_G}^{q(V_{bis} + \phi_{CH})} M(E)T(E) [f_S(E) - f_{CH}(E)] dE. \quad (15)$$

B. Band Tail Effect

In (15), M is the number of the conduction modes, which is associated with the average velocity of the carrier and the density of states (DOS) [23], [24]. Due to the thin body of the device of interest, a 2-D M is adopted and can be written as [23]

$$M(E) = Wg_v \frac{\sqrt{2m^*(E - E_G)}}{\pi \hbar} \quad (16)$$

where W is the device width and g_v is the valley degeneracy. From (16), it is expected that there is no any conduction mode or DOS in the bandgap so that the lower limit of integration (15) is E_G . However, in reality, the band edge is not perfectly sharp [25]. The DOS would extend into the bandgap, called Urbach tail [26], affecting the turn-ON characteristics of TFETs [27]. This effective bandgap states broadening may

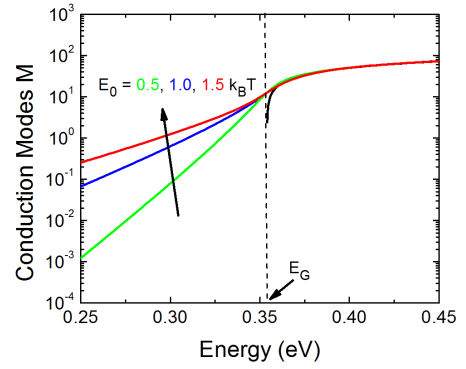


Fig. 5. Conduction modes as a function of energy using InAs material parameters with $W = 1 \mu\text{m}$. Below E_G , it shows tails for various Urbach parameters E_0 .

be caused by the phonon induced tunneling states broadening and doping inhomogeneity. The DOS of the Urbach tail decays exponentially into the bandgap [28]

$$N(E) \propto \exp \left(-\frac{E_G - E}{E_0} \right) \quad (17)$$

where E_0 is the Urbach empirical parameter and is comparable to the room temperature thermal energy, which is always determined by optical measurements [27]. Urbach parameter may be doping-dependent [29], but in the model, it is treated as a fitting parameter in order of magnitude of the thermal energy due to nonuniform doping profile in real devices. To incorporate band tail effect into the TFET compact model, (16) is multiplied by (17). Due to the band states tail, the lower limit of integral in (15) becomes $0.5E_G$ (midgap). Although (17) exponentially decays in the bandgap, limiting (17) not to increase for $E > E_G$ is necessary. This can be numerically solved by replacing the exponential function (17) with an exponential function inside a hyperbolic tangent function, ensuring that when E is large (small), the hyperbolic tangent becomes unity (exponential function). Fig. 5 shows M as a function of energy. The conduction modes due to Urbach band tail lead to additional current at low gate bias but degrade the subthreshold slope, which will be discussed in Section III.

C. Gaussian Quadrature Method

Although the Landauer equation captures the physics appropriately, the problem for a compact model is that the integral of such equation is not easy to carry out analytically. Indeed, most of the studies on TFET modeling obtain drain current models relying on extensive modeling approximations so a close form drain current model can be obtained. Without losing essential physics by making some approximations for the integral, a numerical strategy called Gaussian quadrature method is introduced in this paper. Gaussian quadrature technique states that an integral of an arbitrary well-behaved function can be simply expressed as a summation by choosing specific weights and abscissa [12]. Mathematically, an integral can be

TABLE I
EXAMPLE WEIGHT AND ABSCISSA FOR GAUSSIAN
QUADRATURE FOR $N = 8$

i	Weight w_i	Abscissa ζ_i
1, 2	0.3626837833783620	± 0.1834346424956498
3, 4	0.3137066458778873	± 0.5255324099163290
5, 6	0.2223810344533745	± 0.7966664774136267
7, 8	0.1012285362903763	± 0.9602898564975363

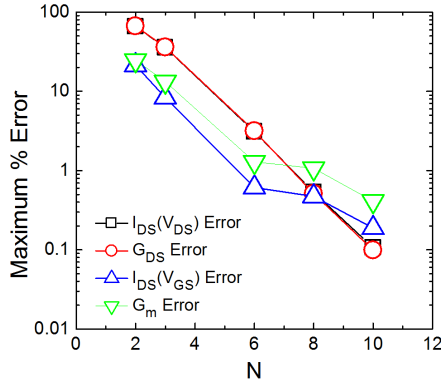


Fig. 6. Maximum % error of $I_{DS}(V_{DS})$, G_{DS} , $I_{DS}(V_{GS})$, and G_m for different numbers of Gauss points.

written as

$$\begin{aligned} \int_a^b f(x)dx &= \int_{-1}^1 f\left(\frac{(b-a)\zeta + (b+a)}{2}\right) \frac{(b-a)}{2} d\zeta \\ &= \int_{-1}^1 F(\zeta)d\zeta \approx \sum_{i=1}^N w_i F(\zeta_i) \end{aligned} \quad (18)$$

where a and b are the upper and lower limits of the integral, N is the number of Gauss points, w_i is the weight, and ζ_i is the abscissa. An example table of w_i and ζ_i for $N = 8$ is shown in Table I. Because Gaussian quadrature involves summation, it is expected that the speed would be slower than a simple analytical equation for the current calculation. However, it is shown that the speed is not a critical issue, since a smaller N gives reasonable accuracy. If function $f(x)$ in (18) is continuous, the integration result is also continuous no matter how many N is used. The accuracy, smoothness, and speed of this method will be discussed in Section III.

III. RESULTS AND DISCUSSION

A. Accuracy, Smoothness, and Speed

For compact model purpose, the accuracy, smoothness, and speed are the key considerations. An optimized N should be obtained since the Gaussian quadrature technique is adopted. Fig. 6 shows the maximum % error of $I_{DS}(G_{DS})-V_{DS}$ and $I_{DS}(G_m)-V_{GS}$ for different N compared to the numerical results, respectively. As expected, more Gauss points reduces error, however, Fig. 7 shows that the CPU time increases linearly with N , because the Gaussian quadrature involves summation for N terms. Gaussian quadrature of $N = 8$ keeps

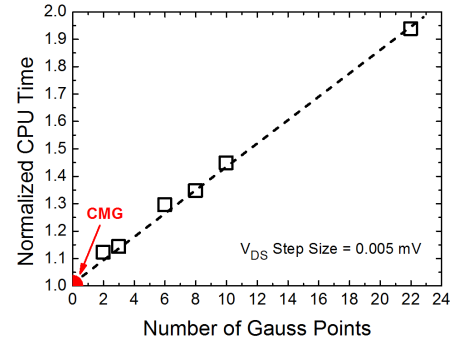


Fig. 7. CPU time versus Gauss points relative to the time used by BSIM-CMG FinFET/NanowireFET model.

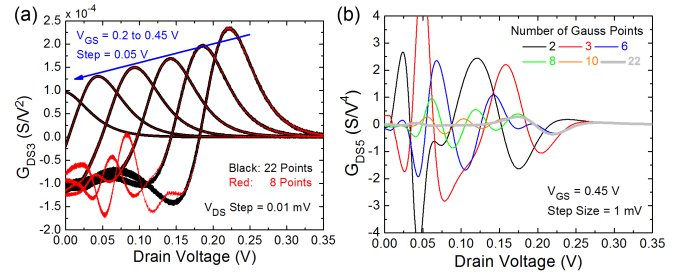


Fig. 8. (a) G_{DS3} for $N = 8$ and 22 with small V_{DS} Step = 0.01 mV. (b) G_{DS5} for various N . High-order derivative of current is smooth using Gaussian quadrature.

the maximum error around 0.5% and only takes 35% more time than the BSIM-CMG FinFET/Nanowire-FET model and appears to be satisfactory. The smoothness of the high-order derivative of current is examined due to its importance in the convergence performance of model. Fig. 8(a) and (b) shows that G_{DS3} (the third-order derivative of the drain current) and G_{DS5} (the fifth-order derivative of the drain current) are smooth even if the step size is very small ($=0.01$ mV) or the number of Gauss points is only 2. Fig. 9 shows the comparison of $I_{DS}(G_{DS})-V_{DS}$ and $I_{DS}(G_m)-V_{GS}$ curves for $N = 8$ and numerical results, indicating that $N = 8$ is good enough for both speed and accuracy requirements. As a result, $N = 8$ will be taken as the default in this TFET compact model.

B. Model Validation

Figs. 10 and 11 show that the model is in good agreement with the $I_{DS}-V_{GS}$ calculated by atomistic simulation for n-TFETs of several different materials and two geometries [30], [31]. The InAs, $\text{Ge}_{0.92}\text{Sn}_{0.08}$, and Ge TFETs have cuboid channel with square cross-sectional area of 25 nm^2 , while the Si TFET has a cylindrical channel with diameter of 3 nm. The material with small bandgap and low electron effective mass has higher drain current due to higher tunneling probability. Effective bandgap states broadening is included in the model to represent the phonon-induced tunneling states broadening, and doping-induced band tail states. The dashed curves in Fig. 10 shows that the turn-OFF characteristic will be sharper than the simulation result if this effect is not included.

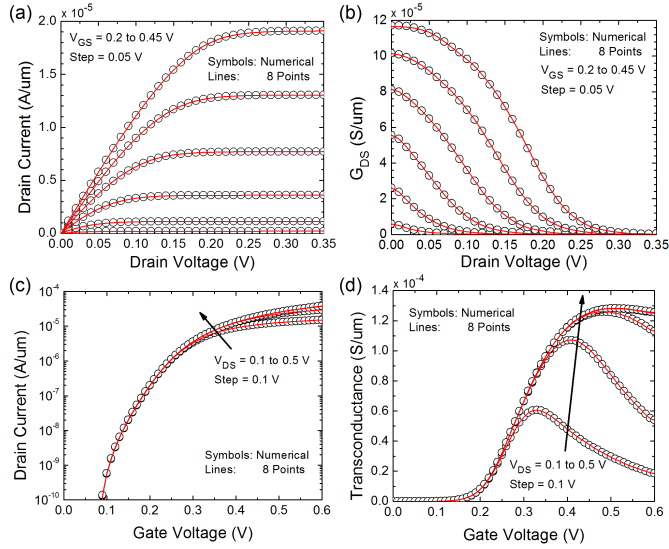


Fig. 9. (a) $I_{DS}-V_{DS}$, (b) $G_{DS}-V_{DS}$, (c) $I_{DS}-V_{GS}$, and (d) G_m-V_{GS} for $N = 8$ and numerical results. There is little accuracy loss in limiting N to 8.

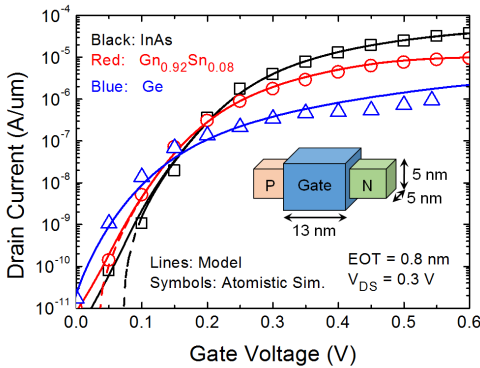


Fig. 10. $I_{DS}-V_{GS}$ of proposed model and atomistic simulations from [30] using various materials. The fin height (HFIN) and thickness (TFIN) are 5 nm. Dashed lines: model without band tail.

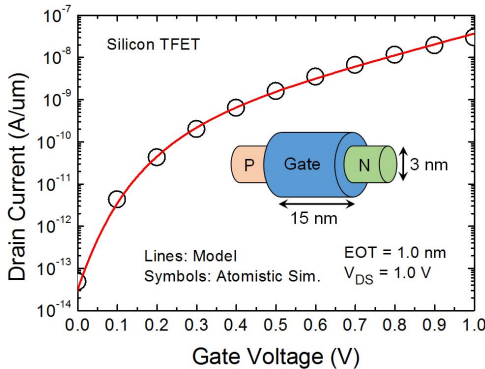


Fig. 11. Silicon TFET $I_{DS}-V_{GS}$ of proposed model and atomistic simulation from [31]. The diameter of the channel is 3 nm.

If the bandgap is wider, the current coming from the band tail becomes smaller due to lower tunneling probability so that in Ge and Si TFETs the band tail effect is not observed from the atomistic simulation data. The parameters used in

TABLE II
MAJOR PARAMETERS USED IN FIGS. 10 AND 11

	InAs	Ge _{0.92} Sn _{0.08}	Ge	Si
E_G [eV]	0.354	0.52 ^[31]	0.661	1.619 ^[29]
m^*/m_0	0.021	0.12	0.12	0.32 ^[32]
N_V [m ⁻³]	6.66×10^{24}	5.00×10^{24}	5.00×10^{24}	1.80×10^{25}
χ [eV]	4.90	4.00	4.0	4.05
ϵ_r	15.15	16.2	16.2	11.9
$1 - R$	0.0444	0.04663	0.03964	0.01114
R_{SD} [$\Omega\mu\text{m}$]	500	400	400	100
W_M [eV]	5.13	4.156	4.06	4.08
E_0 [meV]	39.0	44.2	26.0	26.0
N_S [m ⁻³]	7.00×10^{25}	4.00×10^{25}	2.00×10^{25}	9.00×10^{25}

Material parameters are mainly from [30] unless otherwise specified. The shadowed rows represent the parameters tuned for fitting.

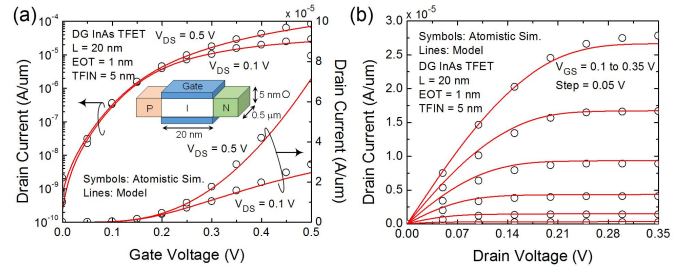


Fig. 12. (a) $I_{DS}-V_{GS}$ and (b) $I_{DS}-V_{DS}$ of an $L = 20$ nm DG InAs TFET with TFIN = 5 nm and EOT = 1 nm. The model exhibits good agreement with the atomistic simulations [3].

the model are listed in Table II. The material parameters are taken from the literatures [31]–[34]. The gate work function W_M , source doping concentration N_S , reflectance R , Urbach parameter E_0 , and R_{SD} are the fitting parameters. Fig.12 shows that the model can not only capture $I_{DS}-V_{GS}$ but also $I_{DS}-V_{DS}$ characteristics of a DG InAs TFET with $L = 20$ nm and TFIN = 5 nm [3]. Therefore, the proposed model can accurately describe the current behaviors with different materials, device geometries, and biases.

IV. CONCLUSION

A predictive TFET compact model is presented. It can capture the WKB-based band-to-band tunneling probability, the electron wave reflectance, and the band tail effect using Landauer equation. Because there is no close form results of integration of Landauer equation, we adopt the Gaussian quadrature method and show that this numerical technique as an accurate, computationally efficient, and smooth technique eminently suitable for compact model. The predictive nature model is validated by atomistic simulation using different materials and device structures.

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