Modeling of Back-Gate Effects on Gate-Induced Drain Leakage and Gate Currents in UTB SOI MOSFETs

Yen-Kai Lin, *Student Member, IEEE*, Pragya Kushwaha, Harshit Agarwal, Huan-Lin Chang, *Member, IEEE*, Juan Pablo Duarte, *Student Member, IEEE*, Angada B. Sachid, *Member, IEEE*, Sourabh Khandelwal, *Member, IEEE*, Sayeef Salahuddin, *Senior Member, IEEE*, and Chenming Hu, *Life Fellow, IEEE*

***Abstract*— The back-gate bias-dependent gate-induced drain leakage (GIDL) and gate current models of ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFETs are proposed. From the experimental data, the GIDL current depends on the back bias due to the electric field change in the channel/drain junction. This effect is modeled using effective gate bias as the threshold voltage shifts. The back-gate bias-dependent gate current is also analyzed and modeled. The voltage across the oxide and available charges for tunneling are the important factors. In accumulation bias condition, the gate leakage is mainly flowing through the overlap region, while in inversion bias condition the current is tunneling from the gate to the channel. Both back bias-dependent GIDL and gate current models are implemented into industry standard compact model Berkeley Short-channel IGFET Model-Independent Multi-Gate for UTB SOI transistors. The model is in good agreement with the experimental data.**

***Index Terms*— Back gate, Berkeley short-channel IGFET model-independent multi-gate (BSIM-IMG), gate leakage, GIDL, modeling, tunneling.**

I. Introduction

ULTRATHIN body (UTB) silicon-on-insulator (SOI) MOSFETs (also known as fully depleted SOI or FDSOI) have been adopted in low static power applications due to suppression of the short-channel effect without using heavily doped body [1], which not only improves carrier mobility for drive current but also minimizes doping-dependent variations in the threshold voltage [2]. In addition, the dynamic threshold voltage control by utilizing back-gate bias (V_{BGS}) is the promising characteristic of UTB SOI MOSFET [3], which is favorable for low-power designs without relying on multiple channel doping concentrations for devices [4]. However, the back-gate bias affects the electrostatics in the thin body, which further alters the carrier concentration and front gate oxide electric field. Thus, the impact of back-gate bias on leakages in UTB SOI MOSFET is distinct and strong as compared with the body effects on leakages in bulk MOSFET [7], [8] and FinFET [9]. The leakages should be accurately modeled in order to evaluate the static power consumption of circuits. In this paper, the mechanism of the back-gate effects on gate-induce drain leakage (GIDL) and the gate leakage is discussed and modeled. The proposed models are incorporated into the industry standard compact model BSIM-IMG [4]–[6], and show good agreement with the experimental data.

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Y.-K. Lin, P. Kushwaha, H. Agarwal, H.-L. Chang, J. P. Duarte, A. B. Sachid, S. Salahuddin, and C. Hu are with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720 USA (e-mail: yklin@berkeley.edu).

S. Khandelwal is with Macquarie University, Sydney, N.S.W. 2109, Australia (e-mail: sourabh.khandelwal@mq.edu.au).

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II. Model Description

A. Gate-Induced Drain Leakage Modeling

Gate-induced drain leakage (GIDL) is the band-to-band tunneling leakage at OFF-state, which strongly depends on the drain voltage [10]. Due to high drain-to-gate voltage ($V_{DG} = V_{DS} - V_{GS}$), an inversion layer is formed in source/drain extension (overlap) region and high electric field leads to band-to-band tunneling, which is typically modeled by [10]

$$I_{GIDL} = \text{AGIDL} \cdot W \cdot E^{\text{PGIDL}} \cdot \exp\left(-\frac{\text{BGIDL}}{E}\right) \quad (1)$$

where W is the device width, AGIDL, BGIDL, and PGIDL are the model parameters which are associate with source/drain material, and E is the electric field in the source/drain overlap region and is given by

$$E = \frac{V_{DS} - V_{GS} + V_{FBSD} - \text{EGIDL}}{\varepsilon_{\text{ratio}} \cdot \text{EOT1}} \quad (2)$$

where V_{DS}, V_{GS}, and V_{FBSD} are the drain voltage, front gate voltage, and flat band voltage of the overlap region, $\varepsilon_{\text{ratio}}$ is the permittivity ratio of the semiconductor to the front gate oxide, *EOT*1 is the effective front gate oxide thickness, and *EGIDL* is the model parameter.

Fig. 1(a) and (b) shows the back-gate bias-dependent GIDL currents of UTB SOI P-MOSFET and N-MOSFET which are fabricated by an industry lab. By Gauss's law, the effects of back-gate bias can be viewed as the threshold voltage shift

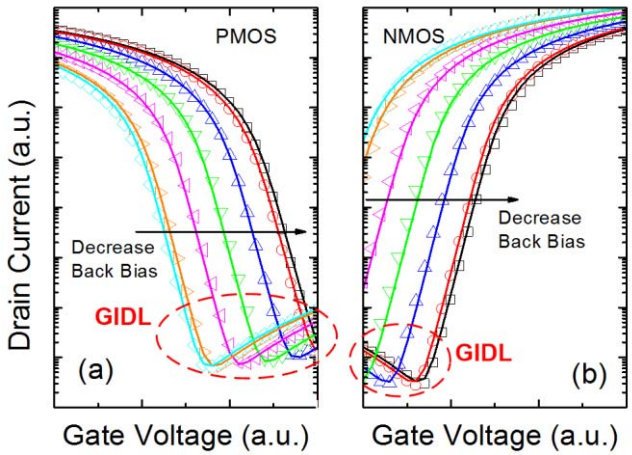

Fig. 1. I_D–V_G characteristics of UTB SOI (a) P-MOSFET and (b) N-MOSFET. The GIDL currents show back-gate dependent behaviors. The lines and symbols represent models with BSIM-IMG and measured data, respectively. The drain is biased at saturation region. Back-gate bias is from positive (left) to negative (right) values.

in the overlap region, which makes V_{GS} in (2) becomes an effective front gate voltage V_{GSeff}

$$V_{GSeff} = V_{GS} - \text{VBGIDL} \cdot \gamma_0 \cdot (V_{BGS} - V_{FBSDBG} - \text{VBEGIDL}) \tag{3}$$

where VBGIDL and VBEGIDL are the model parameters for nonuniform doping in the overlap region, V_{FBSDBG} is the flat band voltage of the overlap region with respect to the back gate, and γ_0 is the capacitive coupling ratio between the body and the back-gate capacitance with the front gate capacitance [11], [12]

$$\gamma_0 = -\frac{C_{Si} \cdot C_{OX2}}{(C_{Si} + C_{OX2}) \cdot C_{OX1}} \tag{4}$$

where C_{Si}, C_{OX2}, and C_{OX1} are the capacitances of the thin body, back gate, and front gate, respectively. The model parameter VBGIDL is around 1, while *VBEGIDL* is on the order of 100 mV. In (4), a fully depleted thin body is assumed so that C_{Si} is a constant ($=\varepsilon_{Si}/T_{Si}$). From (3) and (4), at OFF-state ($V_{GS} < 0$), the magnitude of the effective front gate voltage increases with decreasing (increasing) the back-gate bias for N-MOSFET (P-MOSFET) so that the electric field in (2) becomes higher, giving rise to higher tunneling current. This model is implemented into BSIM-IMG, and the model shows good agreement with the experimental data, as shown in Fig. 1.

B. Back-Gate Bias-Dependent Gate Tunneling Current

As the oxide continuously scales, the gate tunneling gets severe. The gate tunneling currents, including gate-to-channel (I_{gc}) and gate-to-source/drain (I_{gs}, I_{gd}) as shown in Fig. 2, have been modeled [13], [14]. In general, the gate direct tunneling leakage current can be expressed as [13]

$$I_G = W \cdot L \cdot A \cdot \left(\frac{T_{oxref}}{t_{ox}}\right)^{NTOX} \cdot \frac{V_{GS(D)} \cdot V_{aux}}{t_{ox}^2} \cdot \exp[-B \cdot (\alpha - \beta |V_{ox}|) \cdot (1 + \gamma |V_{ox}|) \cdot t_{ox}] \tag{5}$$

where L is the length of tunneling region, A ($=4.97232 \times 10^{-7}$ for N-MOSFET, 3.42537×10^{-7} for P-MOSFET using silicon

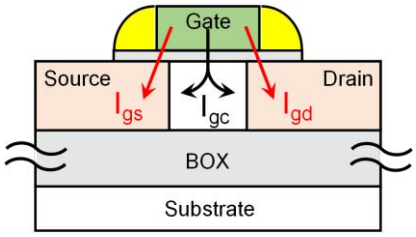

Fig. 2. Schematic of leakage current components. I_{gs} and I_{gd} are the leakage currents at the overlap region. I_{gc} is flowing between the gate and the channel.

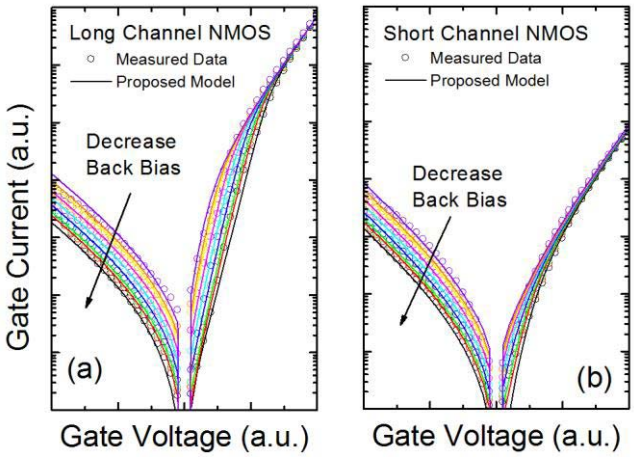

Fig. 3. I_G–V_G characteristics of UTB SOI (a) long- and (b) short-channel N-MOSFETs. The source and drain are shorted when measuring. The ratio of long and short gate length is 100 with the same gate width.

and silicon dioxide parameters) and B ($=7.45669 \times 10^{11}$ for N-MOSFET, 1.16645×10^{12} for P-MOSFET using silicon and silicon dioxide parameters) are the material-related constants, *NTOX*, α, β, and γ are the model parameters, V_{ox} is the oxide voltage, t_{ox} is the physical thickness of the oxide, T_{oxref} is the reference oxide thickness at which all the parameters are extracted, and V_{aux} (in unit of volt) is an auxiliary function which represents the density of tunneling carriers as well as available states. Equation (5) has been widely used in gate currents of planar MOSFETs [13]. However, due to lightly doped thin film used in the state-of-the-art devices, the body effect or back bias effect on gate current characteristic has not received much attention and physics remains unclear [15].

Fig. 3 shows the gate leakage current characteristics of long- and short-channel UTB SOI N-MOSFETs fabricated by an industry lab. The source and drain are shorted when measuring gate current. Note that in Fig. 3 the gate length of long-channel device is 100 times longer than that of short-channel device, while their gate widths are the same. The gate leakage current exhibits V_{BG}-dependence, indicating that the back-gate bias affects the electrostatics in the channel and source/drain overlap regions. Interestingly, the gate leakage current of long-channel device at accumulation regime ($V_{GS} < 0$, left side) is approximately the same as that of short-channel device, implying that the current is flowing through the overlap region whose dimension does not scale with channel dimension [16]. Note that the term "accumulation" used here is for convenience. There is no

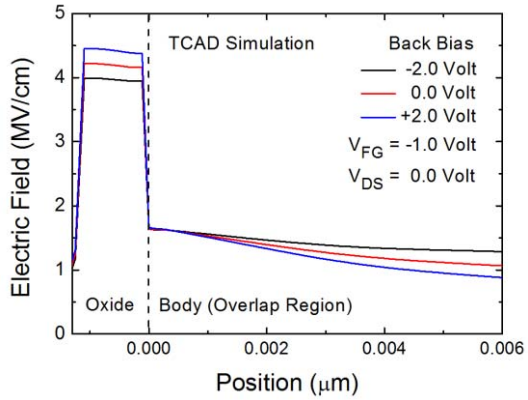

Fig. 4. Simulated electric field at $V_{GS} < 0$ with various back biases in the overlap region. The front gate oxide electric filed increases with back bias.

accumulation layer in UTB SOI device because of insufficient supply of majority carriers from the thin body [17]. Thus, the gate-to-source (I_{gs}) and gate-to-drain (I_{gd}) currents dominate the gate leakage at accumulation region. Because part of the overlap region is heavily doped, the gate-to-overlap region is assumed to be an metal-insulator-metal capacitor, although some lightly doped region is present so that the oxide electric field in the overlap region is affected by the back-gate bias due to the vertical and lateral electric field profile. This assumption means that the gate voltage mostly drops on the oxide and simplifies the auxiliary function. Therefore, based on (5), $|V_{ox}|$ and V_{aux} of gate-to-source (drain) currents can be written as

$$\begin{aligned} &|V_{ox}| \\ &= |V_{GS(D)} - V_{FBSD} - (\phi_{sSD} - \eta \cdot \gamma_0 \cdot (V_{BGS} - V_{FBSDBG}))| \\ &\approx |V_{GS(D)} - V_{FBSD} + \eta \cdot \gamma_0 \cdot (V_{BGS} - V_{FBSDBG})| \end{aligned} \tag{6}$$

and

$$V_{aux} = V_{ox} \tag{7}$$

where η is the model parameters for nonuniform doping in the overlap region. Note that, in (2), the absolute value is taken using the smoothing function in order to avoid the possible discontinuity in the derivative of the current [11]. In (6), ϕ_{sSD} is the band bending in the overlap region without back-gate effect, which is negligible. A negative back-gate bias can raise the band in the overlap region and thus reduce the oxide electric field which is demonstrated by Sentaurus TCAD simulation [18] in Fig. 4. Thus, the gate-to-source (drain) leakages increase with the back-gate bias.

In Fig. 3, at inversion bias region ($V_{GS} > 0$, right side), it is observed that the gate leakage current of long-channel device is 100 times larger than that of short-channel device, which is exactly the same as the ratio of gate lengths of these two devices. This fact implies that the gate-to-channel current (I_{gc}) dominates because it is proportional to the gate length. Note that the gate-to-channel current partition due to the drain voltage has been modeled in BSIM4 [13] and BSIM-IMG [4], which is important when the drain bias is nonzero. At inversion, V_{aux} can be represented as the average charge q_{ia} (in unit of volt) in the channel, which is directly

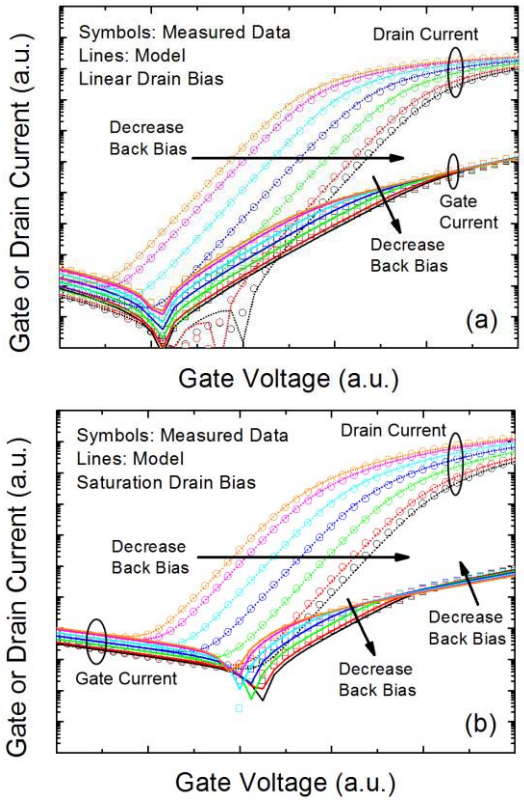

Fig. 5. Gate and drain currents versus gate voltage at various back-gate biases and at (a) linear and (b) saturation drain biases in a long-channel N-MOSFET. The back-gate bias varies from positive to negative values.

calculated by the core model of BSIM-IMG model [4]. V_{ox} can be written as

$$V_{ox} = V_{GS} - V_{FB} - \zeta \cdot \phi_s \tag{8}$$

where ζ is the model parameter to capture nonuniform electric potential along the channel due to drain voltage, V_{FB} is the flat band voltage, and ϕ_s is the surface potential of the front side of body at the source which is V_{BGS} dependent and is determined by the core model of BSIM-IMG model [4]. From (8), ϕ_s decreases with decreasing V_{BGS} [4], [19] so that V_{ox} increases with decreasing V_{BGS}. However, the available charges for tunneling (q_{ia}) exponentially increase with V_{BGS} before the threshold. Thus, the net result is that the gate-to-channel leakage current increases with V_{BGS}. Furthermore, at weak inversion the inversion charges are not abundant, so the back-gate effect is still dominant, giving rise to V_{BGS} dependence. Nevertheless, at strong inversion the inversion charges are able to screen out the back-gate electric field, which means that the back-gate effect becomes less significant. This fact leads that the gate leakage currents at high V_{GS} for various V_{BGS} start to merge [20].

Equations (5)–(8) are implemented into BSIM-IMG model. Fig. 3 shows the model results are in good agreement with the measured data of both long- and short-channel devices. To examine the model, different drain biases are applied for gate currents. Fig. 5 shows the long-channel gate and drain currents versus gate voltage at various back-gate biases at linear and saturation regions. After fitting the drain current

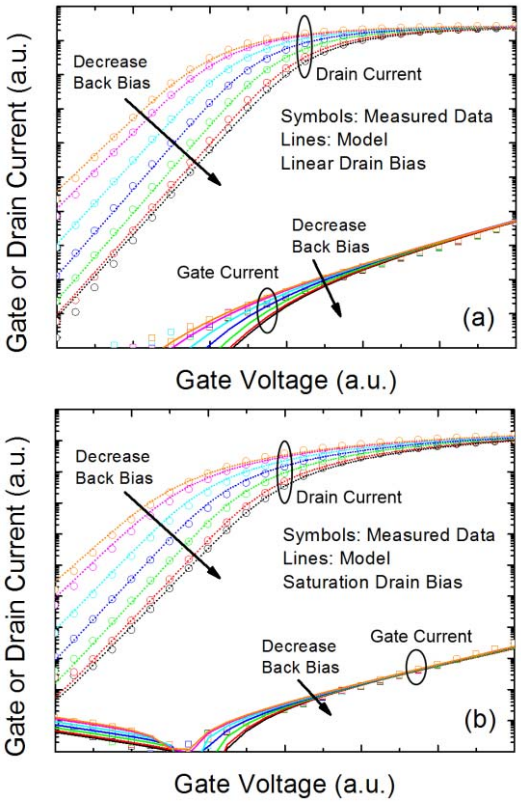

Fig. 6. Gate and drain currents versus gate voltage at various back-gate biases and at (a) linear and (b) saturation drain biases in a short-channel N-MOSFET. The back-gate bias varies from positive to negative values.

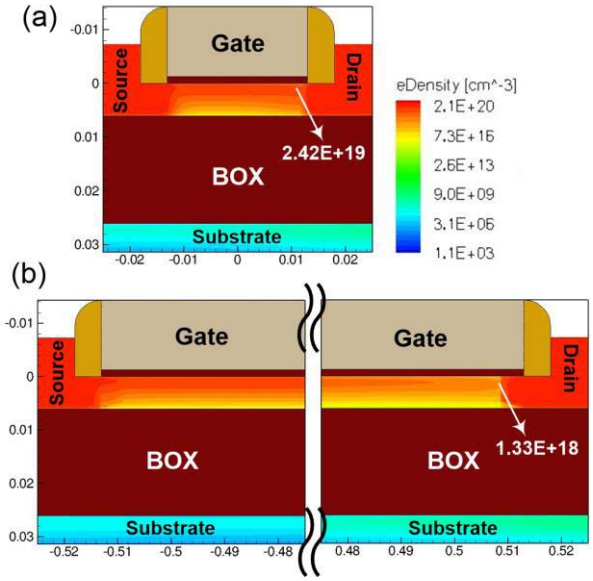

Fig. 7. TCAD simulated electron density in (a) short-channel (~20 nm) and (b) long-channel (~1 μm) devices at $V_{GS} = 1$ V, $V_{DS} = 0.8$ V, and $V_{BGS} = -2$ V. The electron distribution is uniform in short-channel device.

to get accurate q_{ia}, the gate current is fitted. The drain currents of both linear and saturation bias regions at OFF-state ($V_{GS} < 0$, left side) are dominated by the overlap gate current (I_{gs} and I_{gd}) in this device. This leakage current shows opposite V_{BGS} dependence to the GIDL mentioned in Section II-A. This distinct characteristic is helpful for distinguishing the leakage components and is a guideline to reduce leakages. Note that the gate current at saturation bias region shows V_{BGS}-dependence crisscrossing at high V_{GS} because the V_{ox} effect overwhelms q_{ia} effect. The drain voltage would reduce the average charges in the channel as well as the screening effect for the back electric field to the front electric field. Fig. 6 shows the short-channel gate and drain currents. The proposed model also matches the experimental data well. Interestingly, the short-channel gate currents do not show V_{BGS}-dependence crisscrossing at high V_{GS} because the charges are more abundant than that in long channel due to lower threshold voltage. Also, the charge distribution is also more uniform compared to that of long channel, as shown in Fig. 7. Thus, the electric field from the back gate is screened out, leading to less V_{BGS}-dependence but not crisscrossing.

III. Conclusion

The back-gate bias-dependent GIDL and gate current models are developed. It is found that the back bias changes the electric field in the channel/drain junction, giving rise to back bias-dependent GIDL. This effect is modeled by incorporating the threshold voltage shift due to back bias. Furthermore, the physics of gate currents for various back biases is explored. The back bias changes the oxide electric field and charges in the channel, which leads to back bias-dependent gate currents. It is also found that at accumulation region the gate-to-drain (source) current in the overlap region dominates, while at inversion region the gate-to-channel current is the key component. The proposed models are incorporated into BSIM-IMG and show good agreement with the experimental data.

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Yen-Kai Lin (S'15) received the B.S. degree in physics and the M.S. degree in electronics engineering from National Taiwan University, Taipei, Taiwan, in 2013 and 2014, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with the University of California, Berkeley, CA, USA.

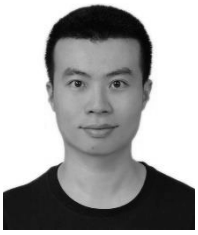
Since 2015, he has been with BSIM Group, University of California. His current research interests include semiconductor devices physics, compact modeling, and simulation.

Pragya Kushwaha received the Ph.D. degree from the Department of Electrical Engineering, IIT Kanpur, Kanpur, India.

She was a Co-Developer of the BSIM compact models. She is currently a Post-Doctoral Researcher with the BSIM Group, University of California, Berkeley, CA, USA. Her current research interests include modeling, simulation and characterization of semiconductor devices such as nanowire, NCFET, PD/FDSOI, FinFET, tunnel FET, high-voltage FET, and bulk MOSFET.

Harshit Agarwal received the Ph.D. degree from IIT Kanpur, Kanpur, India.

He is currently a Post-Doctoral Researcher/Manager with the Berkeley Device Modeling Center, BSIM Group, University of California, Berkeley, CA, USA. His current research interests include modeling and characterization of high-voltage devices, NCFETs, FinFETs, and GAA FETs.



Huan-Lin Chang (S'07–M'11) received the Ph.D. degree in electronics engineering from National Taiwan University, Taipei, Taiwan, in 2011.

He was with SPICE Team, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, from 2011 to 2015. He was a Post-Doctoral Researcher with BSIM Group, University of California, Berkeley, CA, USA. His current research interests include compact modeling of the semiconductor devices.

Juan Pablo Duarte (S'12) received the B.Sc. and M.Sc. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea. He is currently pursuing the Ph.D. degree with the University of California, Berkeley, CA, USA.

Angada B. Sachid (M'11) received the Ph.D. degree in electrical engineering from IIT Bombay, Mumbai, India, in 2010.

He is currently a Post-Doctoral Researcher with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, USA.

Sourabh Khandelwal (M'14) was a Research Engineer with the IBM Semiconductor Research, New Delhi, India. He was a Manager and a Post-Doctoral Researcher with the Berkeley Device Modeling Center, BSIM Group, University of California at Berkeley, Berkeley, CA, USA. He is currently an Assistant Professor with the School of Science and Engineering, Macquarie University, Sydney, NSW, Australia. He is the Lead Developer of ASM-GaN-HEMT compact model for the emerging GaN technology.

Sayeef Salahuddin (SM'14) received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2003, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, USA, in 2007.

He joined the Faculty of Electrical Engineering and Computer Science, University of California at Berkeley, Berkeley, CA, USA, in 2008.

Chenming Hu (LF'16) is currently a Distinguished Professor Emeritus with the University of California at Berkeley, Berkeley, CA, USA. He is also a Board Director of SanDisk Inc., San Jose, CA, USA and Friends of Children with Special Needs, Fremont, CA, USA. He is known for his involvement in FinFET–the 3-D transistor, widely used IC reliability models, and BSIM–the industry standard transistor models used by most IC companies since 1997 to design CMOS products.