Compact Modeling Source-to-Drain Tunneling in Sub-10-nm GAA FinFET With Industry Standard Model

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***Abstract*— We present a compact model for source-to-drain tunneling current in sub-10-nm gate-all-around FinFET, where tunneling current becomes nonnegligible. Wentzel–Kramers–Brillouin method with a quadratic potential energy profile is used to analytically capture the dependence on biases in the tunneling probability expression and simplify the equation. The calculated tunneling probability increases with smaller effective mass and with increasing bias. We at first use the Gaussian quadrature method to integrate Landauer's equation for tunneling current computation without further approximations. To boost simulation speed, some approximations are made. The simplified equation shows a good accuracy and has more flexibility for compact model purpose. The model is implemented into industry standard Berkeley Short-channel IGFET Model-common multi-gate model for future technology node, and is validated by the full-band atomistic quantum transport simulation data.**

***Index Terms*— BSIM-CMG, compact model, FinFET, gaussian quadrature, sub-10 nm, tunneling.**

I. Introduction

CONTINUOUSLY scaling the gate length of MOSFET over 40 years significantly improves the performance of circuit applications. In order to improve gate electrostatic control, a 3-D structure MOSFET, known as FinFET, has been proposed [1]. However, the source-to-drain tunneling (SDT) would be significant in sub-10-nm gate length FinFET due to short tunneling width of channel [2]–[4], which sets a fundamental limit to the device scaling [5]. Although analytical models are given in [5] and [6], the brute force integration in their models are the limitation for the compact model purpose. To evaluate the impact of SDT current on the circuit applications, a compact model of this current component is required. In this paper, the physics of the SDT is explored, and a compact model is proposed using the Gaussian quadrature method [7], [8]. To further boost the simulation speed, the simplification of the equation without the Gaussian quadrature method is carried out. This model is implemented into the industry standard model berkeley short-channel IGFET model (BSIM)-common multi-gate (CMG) and is validated by quantum simulation data [9].

This paper is organized as follows. In Section II, we discuss the detailed physics and model formulation of SDT. The speed comparison of the model using Gaussian quadrature method and the simplified equation is also presented. In Section III, the validation of the developed model and some detailed discussion are made. We conclude this paper in Section IV.

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II. Compact Model Description

A. Intraband Tunneling With Quadratic Potential Barrier

The SDT appears when the potential barrier height and the width of the channel are small enough, i.e., for very short channel length. The drain bias could affect the electrostatics in the channel against the gate so that the potential as well as tunneling probability are drain- and gate-bias dependent. To evaluate the SDT current, the Landauer's equation is adopted [8]

$$I_{\mathrm{SDT}} = \frac{2q}{h}\int M(E)T(E)\left[f_S(E) - f_D(E)\right]dE \qquad (1)$$

where q is the charge, h is the Planck's constant, M is the 2-D conduction mode [8], T is the tunneling probability, and $f_{S(D)}$ is the Fermi distribution function at source (drain). The probability of a carrier to tunnel through a potential energy barrier $V(y)$ can be estimated using Wentzel–Kramers–Brillouin (WKB) approximation

$$T(E) = \exp\left[-\frac{2\sqrt{2m^*}}{\hbar}\int_{y_0}^{y_1}\sqrt{V(y)-K}\,dy\right] \qquad (2)$$

where m^* is the effective mass, $\hbar$ is the reduced Planck's constant, K is the energy of the carrier ($-E$ as defined in Fig. 1), and y_0 and y_1 are defined in Fig. 1 and are the positions where the potential energy is equal to the kinetic energy. Although the WKB approximation (2) may overestimate the tunneling current due to the complex band structure and wave function

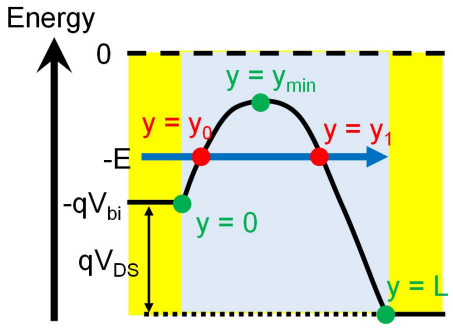

Fig. 1. Electron potential energy profile of a transistor. The yellow and blue regions represent source/drain and channel, respectively.

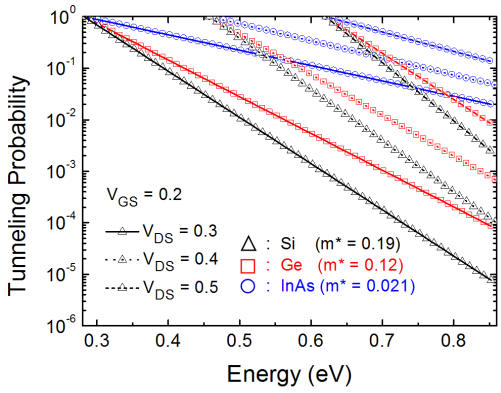

Fig. 2. Calculated tunneling probability versus energy for the device with gate length of 5 nm. The energy ranges from the top to the bottom of the potential barrier.

mismatch at the high field region [9]–[15], for compact model purpose the WKB approximation is used to capture the general dependence on biases and gives a simple analytical equation which is good for the simulation speed. The potential profile in a short channel device can be approximated as a quadratic function [5], as shown in Fig. 1

$$V(y) = a + by + cy^2 \tag{3}$$

with boundary conditions

$$\begin{aligned} V(y=0) &= V_{\text{bi}} \\ V(y=L) &= V_{\text{bi}} + V_{\text{DS}} \\ V(y=y_{\min}) &= V_{\min}. \end{aligned} \tag{4}$$

Hence, three variables a, b, and c are determined

$$\begin{aligned} a &= V_{\text{bi}} \\ b &= -\frac{y_{\min} V_{\text{DS}}}{L(L-y_{\min})} + \frac{L(V_{\min}-V_{\text{bi}})}{y_{\min}(L-y_{\min})} \\ c &= \frac{V_{\text{DS}}}{L(L-y_{\min})} - \frac{V_{\min}-V_{\text{bi}}}{y_{\min}(L-y_{\min})}. \end{aligned} \tag{5}$$

At $y = y_{\min}$, the potential has a local minimum, which gives

$$y_{\min} = L \cdot \sqrt{\frac{V_{\text{bi}}-V_{\min}}{V_{\text{bi}}+V_{\text{DS}}-V_{\min}}} \Bigg/ \left(1+\sqrt{\frac{V_{\text{bi}}-V_{\min}}{V_{\text{bi}}+V_{\text{DS}}-V_{\min}}}\right). \tag{6}$$

In (4), the minimum potential in the channel is expressed as

$$V_{\min} = V_{\text{GS}} - V_{\text{FB}} - V_{\text{OX}} - \Delta V_{\text{th,DIBL}} + \alpha \tag{7}$$

where α is the model parameter to capture nonuniform doping at the source (drain)-to-channel junctions because graded doping may effectively affect the barrier, V_{FB} is the flat band voltage, V_{OX} is the oxide voltage calculated by BSIM-CMG core model which automatically includes the quantum effect [16], and $\Delta V_{\text{th,DIBL}}$ is threshold voltage shift due to drain-induced barrier lowering (DIBL) and is modeled as [16]–[18]

$$\Delta V_{\text{th,DIBL}} = -0.5 \cdot \beta \cdot V_{\text{DS}} / \cosh(\gamma \cdot L/\lambda) \tag{8}$$

where β and γ are the model parameters to increase the model flexibility for various technologies [19], and λ is the characteristic length [18], [20]. The subthreshold swing degradation due to the interfacial quality and electrostatics control is captured in V_{OX} via the gate transfer factor capacitor divider model [16]. Using the analytical expression of the channel potential energy profile, the integration in (2) can be carried out (where the electron is with energy $-E$) and the tunneling probability is

$$T(E) = \exp\left[-\frac{2\sqrt{2m^*}}{\hbar} \cdot \frac{\pi\,(E - qV_{\min})}{2\sqrt{q \cdot c}}\right]. \tag{9}$$

Fig. 2 shows the tunneling probability as a function of energy from the top to the bottom of the channel potential barrier in a device with gate length of 5 nm for different materials: Si, Ge, and InAs. As drain bias increases, the barrier is pulled down and thus the tunneling probability increases. Furthermore, the effective mass also affects the tunneling probability. The carrier with lighter effective mass has more wave nature, which gives higher tunneling probability as predicted in (9). The tunneling probability generally increases exponentially with the energy level from the bottom of the barrier, which is in agreement with the results considering the complex band structure [4]. In Fig. 2, it shows that Si FinFET suffers less SDT and thus has better subthreshold slope [9], although the materials with lighter effective masses and thus higher mobilities are always adopted to boost the current [4], [21]. Note that the same electrostatic potential is assumed for these three materials in Fig. 2 for comparison. At high V_{GS}, the quadratic potential approximation will not be accurate, because the potential barrier from the top toward the drain becomes linear [22]. The tunneling probability with the quadratic potential in this scenario could be overestimated. However, at high V_{GS}, the barrier is low and the tunneling window is narrow so that around the top of barrier the linearity will not affect the total integration much if the quadratic function is assumed.

Based on the energy coordinate system shown in Fig. 1, the upper and lower limit of the integration in (1) is qV_{bi} and $qV_{\min}$. With that, (1) becomes

$$I_{\text{SDT}} = \frac{2q}{h}\int_{qV_{\min}}^{qV_{\text{bi}}} M(E)T(E)\,[f_S(E) - f_D(E)]\,dE \tag{10}$$

and the conduction mode M and Fermi distribution functions are

$$M(E) = W \cdot g_v \cdot \sqrt{2m^*(qV_{\rm bi} - E)}/\pi\hbar$$
$$f_S(E) = \left[1 + \exp\left(\frac{qV_{\rm bi} - E}{k_B T}\right)\right]^{-1}$$
$$f_D(E) = \left[1 + \exp\left(\frac{qV_{\rm bi} + qV_{\rm DS} - E}{k_B T}\right)\right]^{-1} \quad (11)$$

where W is the device width and g_v is the valley degeneracy [8]. Since there is no analytical expression for (10), a numerical technique called the Gaussian quadrature method is introduced to complete the integration [7], [8]. This method states that an integral of a well-behaved function can be expressed as a summation by choosing specific weights and abscissa [23]

$$\int_n^m f(x)dx \approx \sum_{i=1}^{N} w_i f\left(\frac{(m-n)\zeta_i + (m+n)}{2}\right)\frac{(m-n)}{2}$$

where N is the number of Gaussian points, w is the weight, and ζ is the abscissa. The example table of w and ζ can be found in [23]. N in this model is 6, which gives accurate results [8]. By the Gaussian quadrature method, (10) is carried out easily without making further approximations.

B. Simplification of Model Equation

Although the Gaussian quadrature method enables complex integration, however, the speed of the simulation would be reduced, which is undesirable in the case of the tunneling model for compact model purpose. The simplification is required based on some approximations. Due to the drain voltage, the energy level corresponding to the tunneling is far away from the drain Fermi level. Thus, the Fermi distribution of the drain side is assumed to be zero, and the Boltzmann approximation is applied to the source side. Hence, the integration of (10) becomes

$$I_{\rm SDT} \approx \frac{4qWg_v\sqrt{2m}}{h^2}\exp\left[-\frac{\pi q\sqrt{2m}}{\hbar\sqrt{q\cdot c}}(V_{\rm bi} - V_{\rm min})\right] f_{\rm fermi} \times \int_0^{q(V_{\rm bi}-V_{\rm min})} \sqrt{x}\exp\left[-\frac{1}{q}\left(\frac{q}{k_B T} - \frac{q\pi\sqrt{2m}}{\hbar\sqrt{q\cdot c}}\right)x\right]dx \quad (12)$$

where $f_{\rm fermi}$ is to ensure zero current at zero drain bias [24]

$$f_{\rm fermi} = 1 - \frac{2}{1 + \exp\left(qV_{\rm DS}/k_B T\right)}. \quad (13)$$

For Si device with gate length of 5 nm, the coefficient of the exponent in the integration $q/k_B T - q\pi\ (\sqrt{2m/qc})/\hbar$ is much greater than 0, which means that the function in the integration would decrease quickly. Thus, the upper limit of the integration in (12) can be replaced with infinity, so the integration is carried out analytically

$$I_{\rm SDT} \approx \frac{4qWg_v\sqrt{2m}}{h^2}\exp\left[-\frac{\pi q\sqrt{2m}}{\hbar\sqrt{q\cdot c}}(V_{\rm bi} - V_{\rm min})\right] f_{\rm fermi} \times q^{\frac{3}{2}}\left(\frac{q}{k_B T} - \frac{q\pi\sqrt{2m}}{\hbar\sqrt{q\cdot c}}\right)^{-3/2}\frac{\sqrt{\pi}}{2}$$
$$\approx \frac{2qWg_v\sqrt{2m\pi}}{h^2}(k_B T)^{\frac{3}{2}}\exp\left[-\frac{\pi q\sqrt{2m}}{\hbar\sqrt{q\cdot c}}(V_{\rm bi} - V_{\rm min})\right] \times\left(1 + \frac{3\pi\sqrt{2m}k_B T}{2\hbar\sqrt{q\cdot c}}\right) f_{\rm fermi}. \quad (14)$$

For the compact model purpose, (14) is further rewritten as

$$I_{\rm SDT} = A\cdot W\cdot\exp\left[-\frac{B}{\sqrt{c}}(V_{\rm bi} - V_{\rm min})^C\right] \cdot\left(1 + \frac{3V_t B}{2\sqrt{c}}\right)\cdot f_{\rm fermi} \quad (15)$$

where A, B, and C are the model parameters, and V_t is the thermal voltage $k_B T/q$. Fig. 3 shows the comparison of (15) with (10) using the Gaussian integration. Fine-tuning parameters for (15) matches (10) well and has more flexibility which is desirable for compact model purpose. Note that both (10) and (15) are implemented into industry standard model BSIM-CMG. Fig. 4 shows the speed of (10) and (15) compared with BSIM-CMG without SDT model. With simplification, the speed is improved by 5 times (from +16.4% to +3.3%). Therefore, the simplified equation is adopted.

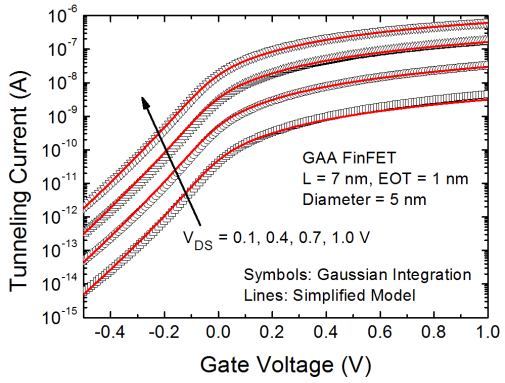

Fig. 3. Comparison of simplified model and Gaussian integration ($N = 6$).

III. Results and Discussion

The model is implemented into industry standard model BSIM-CMG where the simulation results are shown in Figs. 5–7. Fig. 5 shows the SDT current from the model versus $V_{\rm GS}$ for various gate lengths. The SDT current decreases exponentially with the gate length because the bias-dependent function c in (5) is inversely proportional to the gate length square. It can be observed that when the gate length is longer than 10 nm, the SDT becomes less important compared to the normal transistor current. Fig. 6 shows the tunneling current for different drain biases. As the drain bias

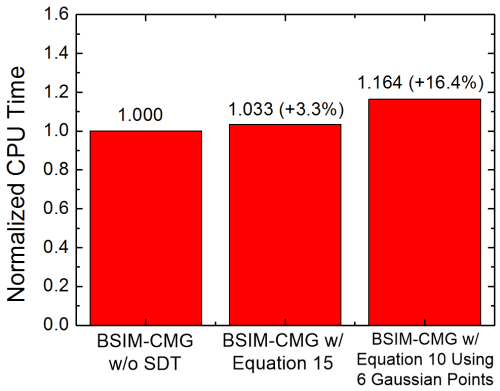

Fig. 4. Speed comparison of BSIM-CMG without and with SDT models.

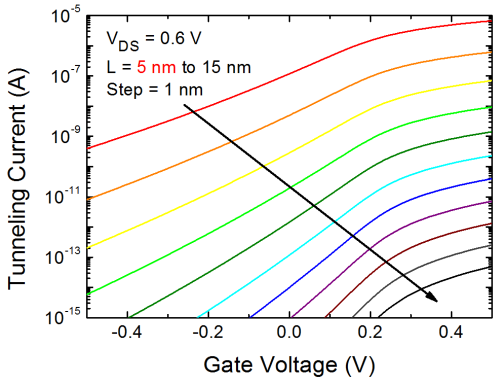

Fig. 5. SDT current versus V_{GS} for gate lengths from 5 to 15 nm in a Si nanowire GAA transistor with diameter of 4 nm and effective oxide thickness (EOT) of 1 nm. The parameters used in simulation are the same as in Fig. 7.

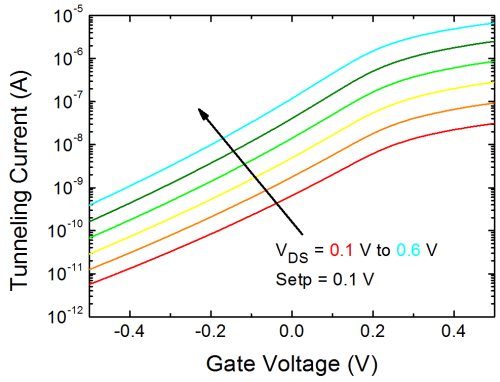

Fig. 6. SDT current versus V_{GS} for V_{DS} = 0.1, 0.2, 0.3, 0.4, 0.5, and 0.6 V in a Si nanowire GAA transistor with diameter of 4 nm, gate length of 5 nm, and EOT of 1 nm. The parameters used in simulation are the same as in Fig. 7.

increases, the potential barrier is reduced and hence boosts the tunneling probability. Fig. 7 shows the model validation with the full-band atomistic quantum transport simulation data of the Si nanowire gate-all-around (GAA) transistors [9]. The extracted model parameters relevant to the SDT current are $A = 1.0023 \times 10^4$ (A/m), $B = 6.15 \times 10^9$ ($m^{-1}V^{-0.5}$), $C = 1.11$, $\alpha = 0.3$ (V), $\beta = 1$, and $\gamma = 0.4$. For $L = 5$ nm, the total current has ~96.3% tunneling current

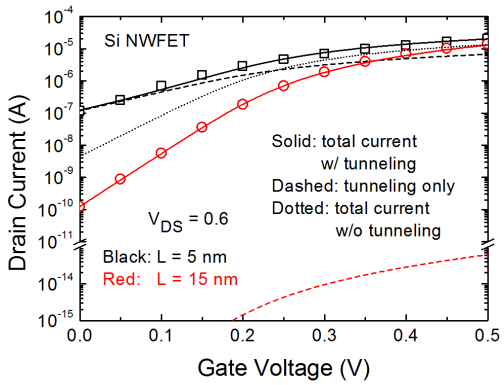

Fig. 7. Drain current versus V_{GS} for gate lengths of 5 and 15 nm in a Si nanowire GAA transistor with diameter of 4 nm. Symbols: simulation from [9]. Lines: proposed model (Solid: total current with tunneling. Dashed: tunneling only. Dotted: total current without tunneling).

at OFF-state ($V_{GS} = 0$ V, $V_{DS} = 0.6$ V) and ~33.5% at ON-state ($V_{GS} = 0.5$ V, $V_{DS} = 0.6$ V), indicating the scaling limit of the transistor. For $L = 15$ nm, the tunneling current is negligible compared to the drift-diffusion current. The subthreshold slope is degraded from 63 to 90 mV/dec as scaling L from 15 to 5 nm. Although the subthreshold slope can be matched using the interfacial capacitance-related parameters [16], there is no reason assuming an ultrascaled device has significantly inferior interfacial quality. The short channel effect could come into the picture when the gate length is scaled [16]. In Fig. 7, the total current without the SDT current is also shown. The subthreshold slope is 78.6 mV/dec, indicating that the short channel effect is insufficient to explain the subthreshold slope degradation. In addition, when scaling the gate length, the fin thickness or even the device geometry will be changed to suppress the short channel effect and improve the subthreshold slope. For example, a tri-gate transistor of 14-nm technology is reported with subthreshold slope of 61 mV/dec [25]. Therefore, the SDT current is a reasonable cause for the subthreshold slope degradation in an ultrascaled device. To extract the model parameters of the SDT current, one may start from the shortest length with good electrostatics control among devices with multiple gate lengths to get accurate model parameters for subthreshold slope degradation due to the short channel effect and interfacial quality. Then, for even shorter gate length device, the model parameters of the SDT current are used to fit the data. For instance, in Fig. 7 the classical subthreshold slope degradation parameters are extracted first from $L = 15$-nm device, and then the SDT current parameters are adjusted to capture the subthreshold region for $L = 5$-nm device.

The hole tunneling from the drain conduction band to the source valence band is neglected. If the bandgap is larger than V_{DS} which is low in ultrascaled FET, this leakage component can be avoided [4]. Although the surface orientation for the transport effective mass would affect the tunneling probability [21], only one effective mass captured by the model parameters is considered to simplify the compact model. Note that in our model the channel length is assumed to be the

same as the gate length. To suppress the SDT, one may use the gate underlap structure to effectively increase the channel length [26], [27] but it may degrade the ON current due to worse series resistance. As a result, the compact model of the SDT is needed to evaluate the circuits using ultimately scaled transistors.

IV. Conclusion

A compact model of the SDT current is presented. The tunneling current is evaluated by Landauer's equation where the conduction modes, WKB-based tunneling probability to capture the essential bias dependence, and Fermi distribution function are considered. Using the Gaussian quadrature technique, Landauer's equation is calculated without approximations. In order to further improve the simulation speed, the formula of the SDT current is simplified. The proposed model is incorporated with the industry standard model BSIM-CMG, and is validated by the GAA FinFET data from the atomistic quantum transport simulations.

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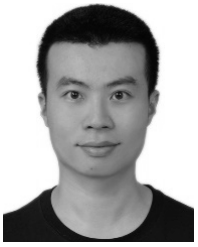

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