Engineering Negative Differential Resistance in NCFETs for Analog Applications

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***Abstract*— In negative capacitance field-effect transistors (NCFETs), drain current may decrease with increasing V_{ds} in the saturation region, leading to negative differential resistance (NDR). While NDR is useful for oscillator design, it is undesirable for most analog circuits. On the other hand, the tendency toward NDR may be used to reduce the normally positive output conductance (g_{ds}) of a short-channel transistor to a nearly zero positive value to achieve higher voltage gain. In this paper, we analyze the NDR effect for NCFET in the static limit and demonstrate that it can be engineered to reduce g_{ds} degradation in short-channel devices. Small and positive g_{ds} is achieved without compromising the subthreshold gain, which is crucial for analog applications. The 7-nm ITRS 2.0 FinFET with 0.7 V V_{dd} is used as the baseline device in this paper.**

***Index Terms*— Analog applications, negative capacitance field-effect transistor (NCFET), negative differential resistance (NDR), sub-60 mv/decade.**

I. Introduction

NEGATIVE capacitance field-effect transistors (NCFETs) [1] have shown promising results in achieving sub-60 mV/decade subthreshold swing (SS). This has been demonstrated over various devices including standard bulk devices and FinFETs [2]–[4]. Such behavior of NCFETs is attributed to internal voltage amplification (w.r.t. applied gate voltage) by the virtue of negative capacitance of the top ferroelectric (fe)-layer. This amplification can simultaneously provide differential gain as well as large signal gain, thereby improving SS as well as the on current. Recent analysis shows that NCFETs can also provide gate voltage-dependent SS, which helps in reducing OFF-current variations [5]. The voltage at the internal node is also controlled by the drain terminal similar to the gate [5]–[9]. This may lead to deamplification of the internal voltage with increasing drain voltage (V_{ds}), and can cause NDR [10]. Amid increasing efforts to understand the impact of various design parameters on overall performance of NCFETs, in this paper we present a detailed analysis on the NDR. NDR is closely associated with the differential gain and therefore it may not be straightforward to optimize it without affecting SS improvement. For example, it is shown in [11] that increasing thickness of fe layer (T_{fe}) although improves SS, at the same time thicker T_{fe} NCFETs becomes more prone to the NDR effect. We demonstrate that NDR can be used to our advantage by engineering it to reduce g_{ds} (output conductance) degradation (due to short channel effects) in sub-10-nm technology node, without sacrificing improvement in SS. This paves the way for very short-channel devices-based NCFETs for analog applications.

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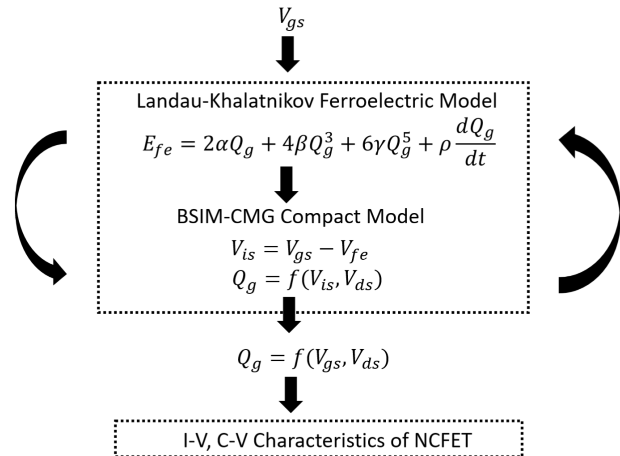

Fig. 1. Modeling of the NCFET using BSIM-common multi gate (CMG) as a core model. This self-consistent model accurately captures the internal voltage (V_{is}) dependence on the gate bias [2] and drain bias as shown in the Appendix.

This paper is organized as follows. In Section II, a framework for a static NCFET modeling and simulation is discussed. Engineering NDR is discussed in Section III. Simulation results are also reported in this section. Conclusion is drawn in Section IV.

II. Compact Modeling and Analysis of NDR

A. Simulation Framework

NCFET is modeled by self-consistently solving electrostatics of the fe layer and FinFET, as shown in Fig. 1. FinFET is

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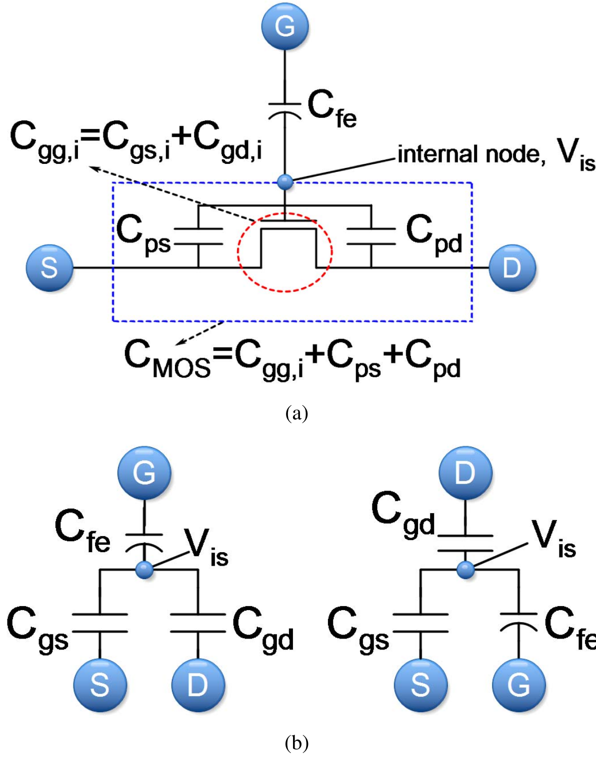


Fig. 2. (a) Equivalent circuit representation for NCFET modeling. (b) Gate and drain control point of view. NDR is due to the coupling between the drain node and internal node. $C_{gs} = C_{gs,i} + C_{ps}$ and $C_{gd} = C_{gd,i} + C_{ps}$.

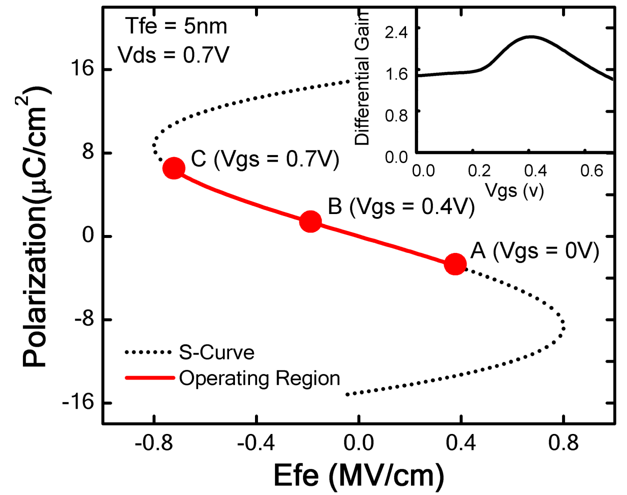


Fig. 3. S-curve of the ferroelectric material. Solid lines shows the operating region for $V_{ds} = 0.7$ V. Points A, B, and C represent position on S-curve for $V_{gs} = 0$, 0.4 and 0.7 V. Inset: differential gain versus V_{gs}. $T_{fe} = 5$ nm, $\alpha = -6.92e10$ cm/F, $\beta = 1.537e20$ cm^5/F/C^2, $\gamma = 0$, and $\rho = 0$. Coercive field $E_c = 0.8$ MV/cm and remnant polarization $P_r = 15\ \mu$ C/cm^2.

modeled by BSIM-CMG model [12], [13], which is the first industry standard model of FinFETs, and ferroelectric layer by the Landau–Khalatnikov (LK) [14] model. This modeling methodology can reproduce experimental NC-FinFET characteristics as demonstrated in [2] and [15]. Voltage and electric field across the ferroelectric (V_{fe} and E_{fe}) are given as [1]

$$V_{fe} = \alpha_0 Q_g + \beta_0 Q_g^3 + \gamma_0 Q_g^5 + \rho \frac{dQ_g}{dt} \quad (1)$$

$$E_{fe} = \frac{V_{fe}}{T_{fe}} = 2\alpha Q_g + 4\beta Q_g^3 + 6\gamma Q_g^5 + \rho \frac{dQ_g}{dt} \quad (2)$$

$$\alpha = \frac{\alpha_0}{2T_{fe}}, \quad \beta = \frac{\beta_0}{4T_{fe}}, \quad \gamma = \frac{\gamma_0}{6T_{fe}} \quad (3)$$

where α, β, and γ are the material parameters [1]. ρ represents the damping in the ferroelectric materials and is neglected in this paper for static analysis. Baseline FinFET is calibrated to ITRS 2.0 7-nm high performance process with gate length $L_g = 14$ nm [16]. Note that, here, we have not considered any extra parasitic capacitance that may result due to the integration of ferroelectric in the gate-stack [6]. The results presented in the subsequent sections qualitatively remain the same under this assumption.

Fig. 2(a) shows the equivalent circuit representation of NCFET [17]. Here, C_{fe} and C_{MOS} represent the capacitances of the fe layer and underlying FinFET, respectively. C_{MOS} is the sum of parasitic capacitance between the internal node and source/drain (C_{ps}/C_{pd}) and the intrinsic capacitance ($C_{gg,i}$) of the FinFET, $C_{MOS} = C_{ps} + C_{gg,i} + C_{pd}$. Fig. 2(b) shows the equivalent circuit of the NCFET from the prospective of gate and the drain control of the internal voltage. Like gate node, drain node is also coupled to the internal node through the capacitor C_{gd}. In that sense, drain acts as a second gate. From Fig. 2(b), differential gain (A_v) and drain-coupling factor (ξ_D) are defined as follows:

$$A_v = \frac{dV_{is}}{dV_{gs}} = \frac{C_{fe}}{C_{fe} + C_{gs} + C_{gd}} = \frac{C_{fe}}{C_{fe} + C_{MOS}} \quad (4)$$

$$\xi_D = \frac{dV_{is}}{dV_{ds}} = \frac{C_{gd}}{C_{fe} + C_{gs} + C_{gd}} = \frac{C_{gd}}{C_{fe} + C_{MOS}}. \quad (5)$$

For hysteresis free operation, $C_{fe} + C_{MOS} \leq 0$ for all the operating bias range [18]. This leads to $A_v > 0$ and $\xi_D < 0$. In Fig. 3, the S-curve of the ferroelectric material along with operating region for $V_{ds} = 0.7$ V, and $V_{gs} = 0$ to 0.7 V is shown. Inset of Fig. 3 shows the differential gain A_v as a function of V_{gs}. Note that, the OFF-state operating point "A" is located in the positive E_{fe} region, which implies that the internal voltage ($V_{is} = V_{gs}$-V_{fe}) is negative at $V_{gs} = 0$ V, leading to lower OFF-current [5], [19]. Interestingly, "A" lies in the negative capacitance region, and therefore $A_v \geq 1$ is achieved as seen from Fig. 3 [5].

B. Analysis of NDR

In order to understand the impact of drain voltage, consider the derivative of drain current which can be expressed using the chain rule [20]–[22] as

$$I_{ds} = f(V_{is}, V_{ds}) \rightarrow \frac{dI_{ds}}{dV_{ds}} = \frac{\partial I_{ds}}{\partial V_{is}} \frac{dV_{is}}{dV_{ds}} + \frac{\partial I_{ds}}{\partial V_{ds}} \quad (6)$$

$$g_{ds} = g_{m,i} \cdot \xi_D + g_{ds,i} \quad (7)$$

where $g_{m,i}$ and $g_{ds,i}$ represent transconductance and output conductance of the internal FinFET, evaluated at amplified gate voltage. For example, if applied gate voltage is 1 V and resulting internal voltage is 1.2 V, then $g_{m,i}$ and $g_{ds,i}$ are the same as the transconductance and output conductance of the

baseline device evaluated at $V_{gs} = 1.2$ V. Note that, g_{ds} in [9] and [23] is defined as $\partial I_{ds}/\partial V_{ds}$, and therefore the expression contains only the first term of (7). Furthermore, since both $g_{m,i}$ and $g_{ds,i}$ are positive (neglecting the self-heating effect [24], [25]), the only factor that can lead to negative g_{ds} in (7) is ξ_D as $\xi_D < 0$ for hysteresis free operation. From (7), condition for positive g_{ds} can be expressed as

$$\frac{g_{m,i}}{g_{ds,i}} \leq \frac{1}{|\xi_D|}. \tag{8}$$

Now consider the operation in linear region, $0 \leq V_{ds} \leq V_{ds,sat}$, where $V_{ds,sat}$ is the drain saturation voltage. In simplified form, drain current of the baseline transistor can be expressed as

$$I_{ds} \approx K_n(V_{is} - V_{th})V_{ds} = K_n.V_{is,ov}.V_{ds} \tag{9}$$

$$g_{m,i} = K_n.V_{ds}; \quad g_{ds,i} = K_n.V_{is,ov} \Rightarrow \frac{g_{m,i}}{g_{ds,i}} = \frac{V_{ds}}{V_{is,ov}} \tag{10}$$

where $V_{is,ov}$ is the gate overdrive voltage, V_{th} and K_n represent the threshold voltage and transistor gain factor, respectively. In the linear region, $V_{ds} < V_{is,ov}$ and $(g_{m,i}/g_{ds,i})$ itself is a small quantity, therefore, condition (8) is easily met. This makes overall g_{ds} positive in (7). As $g_{m,i}$ increases and $g_{ds,i}$ decreases when V_{ds} increases, this may violate the positive g_{ds} condition (8), leading to NDR. Physically, as V_{ds} increases in linear region, two competing effects come into play. First is the reduction of the internal gate voltage, whose effect is to reduce the drain current. Second, the lateral field increases with V_{ds} which increases I_{ds}. Usually the second effect dominates and I_{ds} increases with V_{ds} in the linear region. In the saturation region, although I_{ds} does not depend on V_{ds} for ideal long channel device, however, real short channel devices have dependence due to drain-induced barrier lowering (DIBL) and other short-channel effects (SCE). DIBL is weaker in FinFETs as compared to standard Bulk devices due to better gate control, and is expected to be even better in gate all around (GAA) devices (reported DIBL: 42 mV/V for silicon nanowire [26], 32 mV for nanosheets [27]). Since $g_{ds,i}$ is small and finite in the saturation region, even smaller $|\xi_D|$ can cause negative g_{ds} [see (7)].

III. Engineering NDR

NDR can be optimized by engineering drain-coupling factor in (5). It depends on two key factors: 1) capacitance matching between the ferroelectric capacitor and the underlying FinFET [denominator of (5)] and 2) capacitive coupling between gate-drain, C_{gd}. We will discuss the impact of both these factors. First, consider the capacitance matching. Better the capacitance matching between the C_{fe} and C_{MOS}, smaller would be the denominator in (5) and ξ_D would be large. For a given baseline transistor capacitance C_{gd}, ξ_D can be reduced by increasing $|C_{fe}|$ as it will reduce capacitance matching. C_{fe} depends on the ferroelctric layer thickness and on the slope of S-curve, and can be increased by reducing T_{fe} or E_c or by increasing P_r. The impact of C_{fe} scaling due to T_{fe} is shown in Fig. 4(a) which shows $|g_{ds}|$ for $T_{fe} = 5, 4, 3$, and 2 nm. For all the T_{fe} values except 2 nm, $|g_{ds}|$ has kink in the saturation region, which indicate that g_{ds} is changing sign from positive to negative. The point where g_{ds} become negative shifts to the

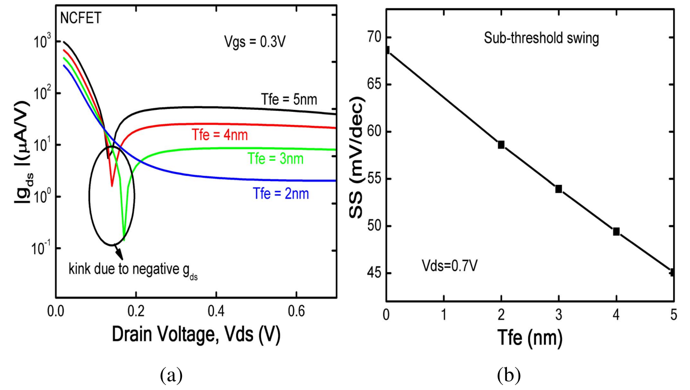


Fig. 4. Designing T_{fe} for NDR optimization. (a) $|g_{ds}|$ vs V_{ds} (b) SS vs T_{fe}. Reducing T_{fe} increases $|C_{fe}|$ and matching between FinFET and ferroelectric capacitance degrades. As a result, NCFET does not show NDR, however, SS also degrades as T_{fe} is scaled down.

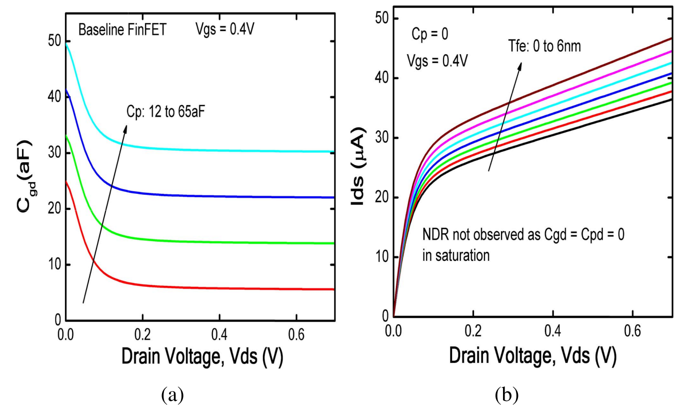
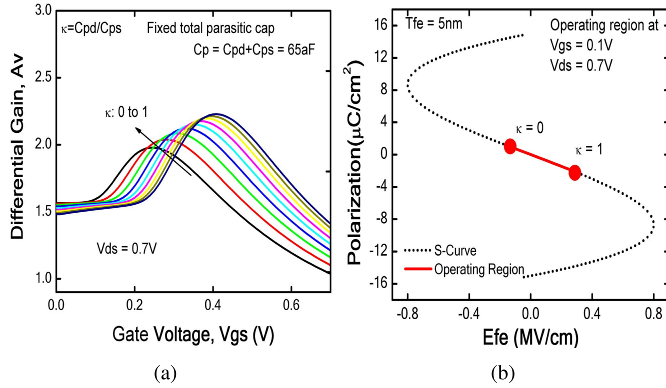


Fig. 5. Understanding the role of parasitic capacitance. (a) C_{gd} as a function of V_{ds} for different parasitic capacitance values of a baseline FinFET. In saturation, $C_{gd} \approx C_{pd}$. In the NCFET, internal node is coupled to the drain node through C_{gd}. Lower C_{gd} in saturation is desired to minimize NDR. (b) I_{ds}-V_{ds} of the NCFET at $V_{gs} = 0.4$ V for $C_p = 0$ case. As C_{gd} becomes very small in the saturation, NDR is not observed even for thick ferroelectric layer.

higher V_{ds} as T_{fe} reduces. For our case, $T_{fe} = 2$ nm does not give negative g_{ds}.

There is an important tradeoff associated with T_{fe} scaling. Differential gain also strongly depends on the capacitance matching [see (4)] and it reduces as T_{fe} is reduced. SS of the NCFET is given as $SS = (1/A_v) * SS_i$ (SS_i: baseline transistor SS) [5], and it degrades with the T_{fe} scaling as shown in Fig. 4(b). Similar behavior with T_{fe} is also reported in [11], where 40-nm T_{fe} is used for analog performance analysis as it does not give NDR, however, it has only 1.07× improvement in SS (88–82 mV/dec).

The other design parameter to optimize NDR is $C_{gd}(= C_{gd,i} + C_{pd})$. Gate charge of the intrinsic transistor is a weak function of the drain potential in saturation region [28] and net capacitance between the gate and the drain node reduces to the parasitic capacitance, $C_{gd} \approx C_{pd}$. This is illustrated in the Fig. 5(a) which shows C_{gd} vs V_{ds} of a baseline FinFET transistor for different cases of parasitic capacitance, $C_p(= C_{ps} + C_{pd})$ while keeping everything else the same in the model [17]. If the parasitic capacitances are minimized such that there is minimal coupling between the gate and drain,



(a) (b)

Fig. 6. Impact of the source and drain parasitics. The total C_p is fixed and ratio of C_{pd} to C_{ps} is varied, $\kappa = (C_{pd}/C_{ps})$. (a) Differential gain versus gate voltage (b) Position in the S-curve at $V_{gs} = 0.1$ V and $V_{ds} = 0.7$ V. Operating point remains in the negative capacitance region for different values of κ. Since total C_p is the same, A_V is nearly the same in subthreshold region.

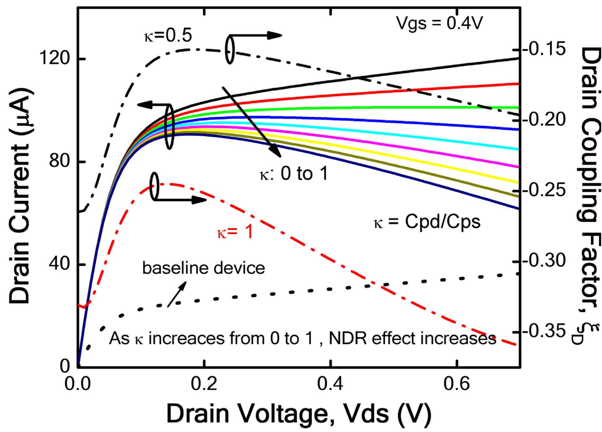


Fig. 7. Impact of source and drain parasitics: I_{ds}-V_{ds} for different $\kappa = (C_{pd}/C_{ps})$. Total C_p is fixed. As κ reduces from 1 to 0, NDR progressively reduces.

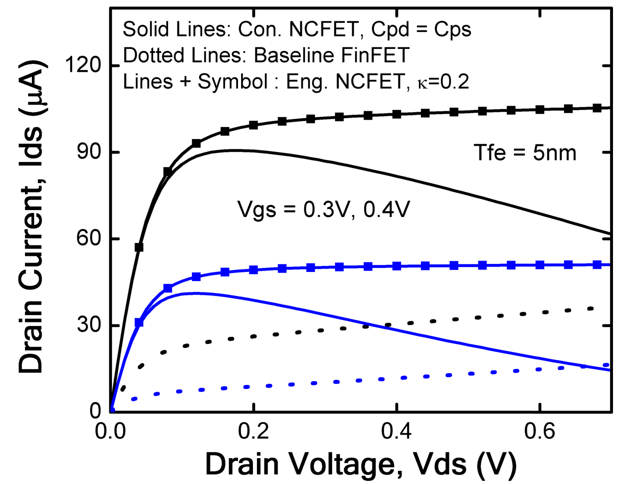


Fig. 8. Output characteristics of an engineered NCFET. In conventional NCFET with symmetric parasitic, current reduces with increasing drain voltage.

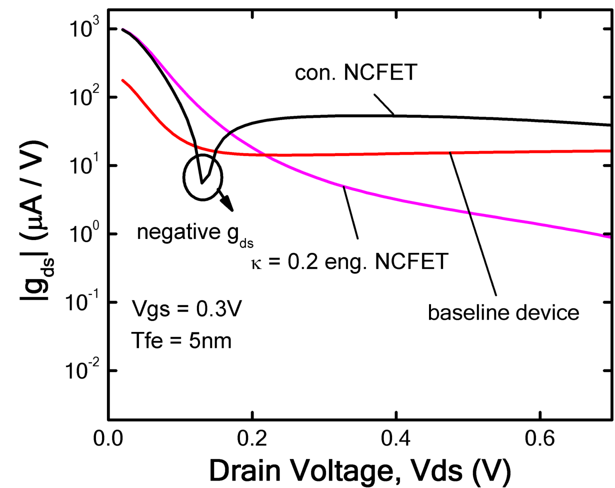


Fig. 9. Engineered NCFET: output conductance, $|g_{ds}|$ versus drain voltage for $\kappa = 0.2$.g_{ds} is always positive for engineered NCFET, while conventional NCFET evince NDR. It is possible to achieve small and positive g_{ds} by using asymmetric source/drain parasitic capacitances. $T_{fe} = 5$ nm.

NDR can be avoided or delayed. To emphasize the importance of coupling, C_p is set to 0 in the compact model and I_{ds}–V_{ds} is simulated for various cases of T_{fe} in Fig. 5(b). Note that, the NDR is not observed. However, similar to the case of T_{fe}, parasitic capacitance also affect the differential gain. In the subthreshold region, $C_{MOS} = C_{gg,i} + C_p \approx C_p$ and A_v in (4) reduces to $(C_{fe}/C_{fe} + C_p)$. Lowering C_p deteriorate the capacitance matching and hence A_v suffers [29].

High differential gain without NDR can be achieved if we attain a good capacitance matching at reduced gate-drain coupling. For this, we analyze the impact of asymmetric parasitic capacitance, i.e., $C_{ps} \neq C_{pd}$. By reducing C_{pd} and increasing C_{ps}, total C_p $(= C_{ps} + C_{pd})$ can still be large to give desired A_v, at the same time coupling between the drain and the gate will be reduced. This is illustrated in Fig. 6(a), which shows A_v for different values of $\kappa = (C_{pd}/C_{ps})$, with total $C_p = C_{pd} + C_{ps}$ constant. Fig. 6(b) shows operating point in the S-curve at $V_{gs} = 0.1$ V and $V_{ds} = 0.7$ V. With reduced drain–gate coupling at smaller κ, the operating point move to the higher polarization state. In the subthreshold region, $A_v \approx (C_{fe}/C_{fe} + C_p)$ is nearly the same for all the values of κ, small change in it is due to the change in C_{fe}, as operating point has changed. Note that in the simulations, only parasitic capacitance are modified by κ, and intrinsic capacitance $C_{gg,i}$ remains the same.

Fig. 7 shows I_{ds}–V_{ds} at different κ for $V_{gs} = 0.4$ V. As κ reduces from 1, the beginning of NDR progressively shifted to the larger V_{ds}. This happens due to the fact that drain-coupling factor in (5) is lowered as κ is reduced, which is also shown in the Fig. 7 for two cases of $\kappa = 1$ and 0.5. In fact, κ can be engineered such that NDR balances out SCE on g_{ds} in the short-channel baseline device, so that small and positive g_{ds} is attained. Fig. 8 shows output characteristics of the baseline FinFET, conventional NCFET with $\kappa = 1$ and NCFET with $\kappa = 0.2$. Total parasitic capacitance is the same in all the cases. The engineered NCFET does not show negative g_{ds}, which is evident from the Fig. 9. Moreover, it offers much lower g_{ds} as compared to the baseline device, which is desirable for analog

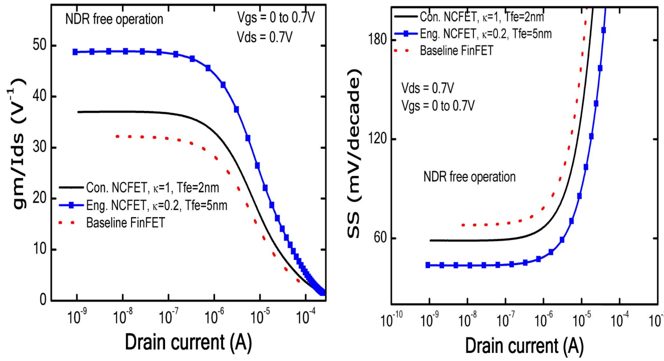


Fig. 10. Performance comparison of NCFET (a) g_m/I_{ds} versus drain current (b) SS versus drain current. Engineered NCFET shows higher transconductane efficiency as well as improved SS than the conventional NCFET and baseline device.

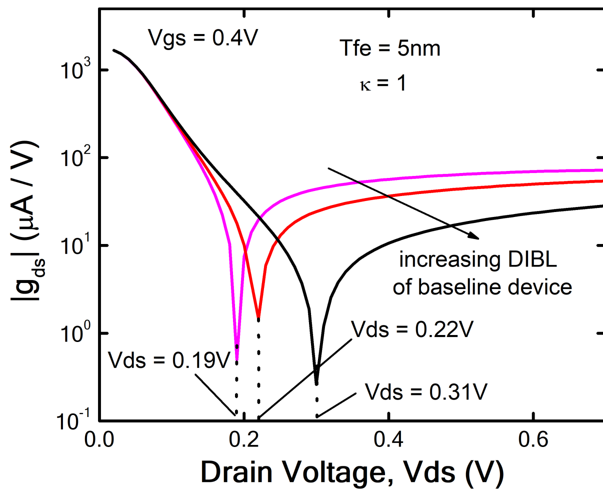


Fig. 11. Output characteristics of the NCFET for different cases of DIBL of the baseline transistor. Larger DIBL results in larger $g_{ds,i}$ of the baseline device, therefore, drain voltage at which g_{ds} becomes negative shifts to higher value. $V_{gs} = 0.4$ V and $\kappa = 1$.

transistors as it increases the intrinsic gain (g_m/g_{ds}) [30]. Therefore, properly designed NCFET can inherently boost the output resistance, without restoring to circuit level techniques [31], [32].

Another important performance metric of the analog transistor is transconductance efficiency (g_m/I_{ds}) [33]. In general, large g_m is required at lower drain current. Fig. 10(a) compares (g_m/I_{ds}) of the engineered NCFET with conventional NCFET (with $T_{fe} = 2$ nm) and baseline FinFET. The engineered NCFET has higher (g_m/I_{ds}) than the conventional NCFET, since its differential gain is high. Fig. 10(b) compare SS of engineered, conventional NCFET and baseline FinFET. As expected, engineered NCFET has much lower SS over the others. This is significant improvement since high (g_m/I_{ds}), small positive g_{ds} and better SS are simultaneously achieved, which certainly makes NCFET a better analog transistor.

Before concluding, consider (7) again. The g_{ds} of NCFET depends on the output conductance and transcounductance of the intrinsic transistor. For a baseline device with strong SCE, $g_{ds,i}$ may be high so that condition (8) remains satisfied for higher V_{ds}. Therefore, different devices (Bulk, FinFET,

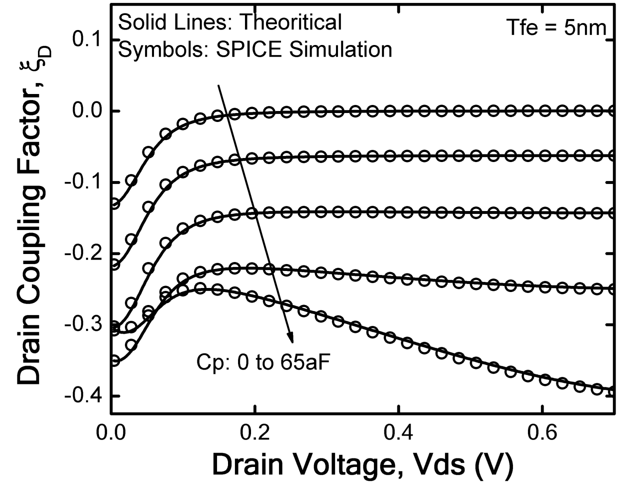


Fig. 12. Coupling factor (ξ_D) versus drain voltage for various values of parasitic capacitance. Symbols represent the values obtained by SPICE simulations and solid lines represents the qualitative model in Fig. 2. The compact model accurately captures drain bias dependence of internal gate voltage.

and GAA) or processes may give different NDR characteristics. To demonstrate this effect, Fig. 11 compares $|g_{ds}|$ of NCFET for different cases of DIBL of the baseline device. Everything is kept the same and only DIBL parameter of the baseline device is changed. Larger the DIBL, V_{ds} at which g_{ds} becomes negative shifts to the higher V_{ds}.

IV. Conclusion

In this paper, we discussed the mechanism of NDR in NCFETs in static limit. A mathematical formulation is presented which suggest that it strongly depends on transconductance and output conductance of the baseline transistor, capacitance matching between the ferroelectric layer and the underlying MOS transistor along with drain–gate coupling capacitor. While a good capacitance matching is desirable for better SS, it may lead to NDR if not properly designed. We also discussed an alternative method of using asymmetric parasitic capacitance at source and drain, which can provide NDR free operation as well as good SS improvement. Simulation shows that this device can give lower g_{ds} and higher (g_m/I_{ds}) at lower current as compared to baseline FinFET and conventional NCFETs. Well-engineered NCFETs will be significantly better analog transistors than the non-NC baseline transistors.

Appendix

The NCFET model in Fig. 1 accurately captures the gate bias dependence [2], [15]. Here, we show that the model also properly accounts for the drain voltage dependence of the internal node voltage. Consider the following:

$$V_{is} = V_{gs} - V_{fe} = V_{gs} - \left(\alpha_0 Q_g + \beta_0 Q_g^3 + \gamma_0 Q_g^5\right) \quad (11)$$

$$\frac{dV_{is}}{dV_{ds}} = -\left(\alpha_0 + 3\beta_0 Q_g^2 + 5\gamma_0 Q_g^4\right).\frac{dQ_g}{dV_{ds}} = -\frac{1}{C_{fe}}.\frac{dQ_g}{dV_{ds}} \quad (12)$$

$$Q_g = f(V_{\text{is}}, V_{\text{ds}}); \quad \frac{dQ_g}{dV_{\text{ds}}} = \frac{\partial Q_g}{\partial V_{\text{is}}}\frac{dV_{\text{is}}}{dV_{\text{ds}}} + \frac{\partial Q_g}{\partial V_{\text{ds}}} \tag{13}$$

$$\frac{dV_{\text{is}}}{dV_{\text{ds}}} = \frac{C_{\text{gd},i}}{C_{\text{fe}} + C_{\text{MOS}}}. \tag{14}$$

Equation (14) is consistent with the qualitative picture in Fig. 2. Fig. 12 compares $(dV_{\text{is}}/dV_{\text{ds}})$ as a function of drain voltage obtained by probing the internal gate voltage during NCFET simulations (symbols) with the one obtained from capacitance ratio in Fig. 2. Note that, coupling factor is negative for hysteresis-free operation.

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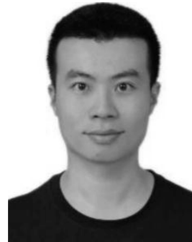

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