Improved SPICE Macromodel of Phase Change Random Access Memory

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ABSTRACT

This paper presents an improved SPICE macromodel of phase change random access memory (PCRAM). Based on the circuit-based model architecture in [1], the novelty of this work lies in (1) accurate modeling the current-voltage (*I-V*) plot including the snap-back phenomenon, and (2) solution to the falling edge problem to avoid misrepresentation of the PCRAM state, and (3) calibration of the crystallization time for potential multilevel (ML) operation of the PCRAM.

I. INTRODUCTION

The past decade has witnessed a heated competition between various next-generation nonvolatile memory (NVM) technologies, including ferroelectrical RAM (FeRAM), magnetoresistive RAM (MRAM), resistive RAM (RRAM), and phase change RAM (PCRAM), all with the aim to replace mainstream flash memory, which is faced with stringent challenges because of the scaling limitation. Among these competitors, PCRAM boasts fast programming speed (comparable with DRAM) and good scalability due to its simple structure. Also, the low-power operation of the PCRAM has the advantage of high-volume memory array integration.

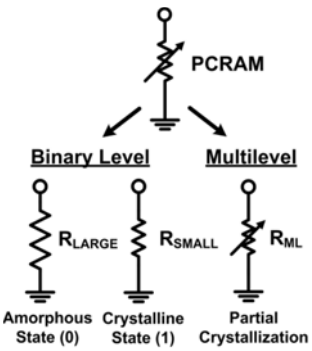


Fig. 1. Binary level and multilevel operation of PCRAM.

In essence, the PCRAM is operated as a variable resistor (Fig. 1). The resistance value depends on which one of the two stable phases (states) the PCRAM is under. If a PCRAM is under the amorphous state, its resistance is large and can, for example, represent a logic 0. Similarly, if a PCRAM is under the crystalline state, its resistance is small and can represent a logic 1. Moreover, a single PCRAM cell can represent more than one bit with partial crystallization, i.e., multiple states can be realized with each state having different resistance values. This promising ML operation can effectively enlarge memory capacity for a given size of memory array. To manipulate the phase change process, current pulses of different amplitudes and durations are applied to the PCRAM cell, resulting in the temperature characteristic as shown in Fig. 2. To change from crystalline to amorphous state, a current pulse with higher amplitude and shorter duration (RESET pulse) is applied to raise the temperature over the melting point (T_M). To change from amorphous to crystalline state, a current pulse with lower amplitude and longer duration (SET pulse) is applied to raise the temperature only over glass transition point (T_{GT}). For a $Ge_2Sb_2Te_5$ (GST)-based PCRAM, T_M is higher than 600℃ and T_{GT} is about 200 ℃.

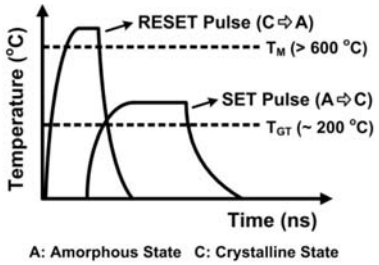


Fig. 2. Temperature characteristic of the phase change process.

While much effort is spent on manufacturing reliable PCRAM, it is of same importance to have a simple and compact model that can accurately characterize its electrical behavior. One of the approaches is to extensively utilize mathematical equations and decision-making codes to handle the phase change process [2]. Another method is to develop a numerical model by the semiconductor device solver [3]. Although behavioral modeling is suitable here, it is hazardous in terms of model scalability and SPICE compatibility without using any circuit components. As for the circuit-based SPICE model [1], [4], [5], the attractive work by Wei et al. [1] combines the advantages of efficient behavioral modeling and scalable circuit components. However, the model of their paper fails to demonstrate the *I-V* plot, which is the most fundamental characteristic of the PCRAM. Also, two critical problems occur in the phase change circuit of the macromodel. Our paper resolves these problems with more robust model architecture.

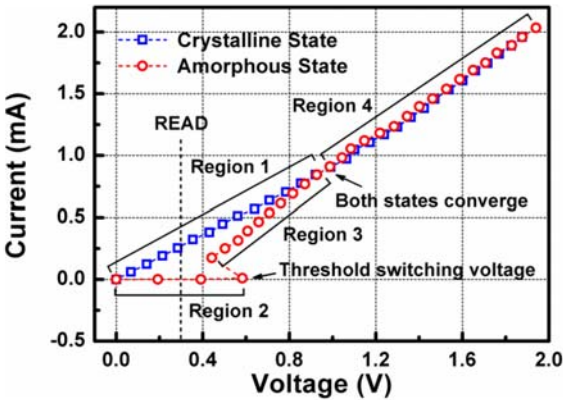


Fig. 3. Measured current-voltage (*I-V*) plot of the PCRAM.

II. ELECTRICAL CHARACTERISTICS

The electrical characteristics of the PCRAM can be evaluated by the current-voltage (*I-V*) plot and the resistance-current (*R-I*) plot. Careful observation of the measured *I-V* and *R-I* plots proves useful in the subsequent modeling process. In the measured *I-V* plot (Fig. 3), it can be seen that the crystalline state (blue square) and the

amorphous state (red circle) form a closed curve, which can be separated into four regions. Region 1 and Region 2 are the low-resistance (crystalline) state and the high-resistance (amorphous) state of the PCRAM. When the voltage applied to the amorphous PCRAM is higher than the threshold switching voltage (~ 0.6 V), a property called ovonic voltage switching (OVS) will happen, lowering the resistance to a much smaller level (Region 3). This turnaround phenomenon of the amorphous *I-V* curve is called 'snapback.' When the applied voltage is high enough (> 1 V), the resistance will converge to the same value for both states (Region 4). To READ the memory, a low voltage (0.3V) is applied to the PCRAM to read the current outputs. The high current represents a logic 1 and the low current represents a logic 0.

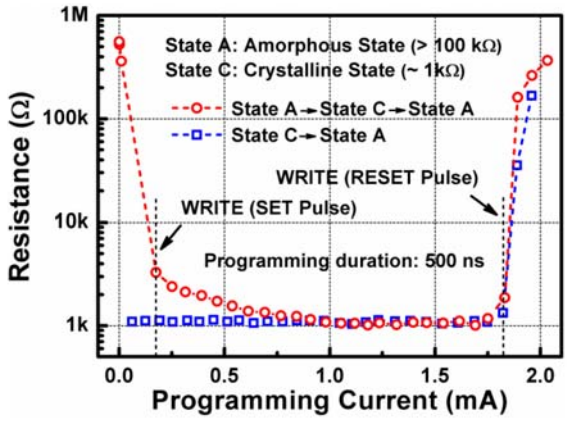


Fig. 4. Measured resistance-current (*R-I*) plot of the PCRAM.

The measured *R-I* plot (Fig. 4) shows the resistance change of the PCRAM when varying the programming amplitude. The programming duration is fixed at 500 ns in this measurement. The resistance ratio between the amorphous state (> 100 kΩ) and the crystalline state (~ 1 kΩ) is larger than 100, which makes ML operation of the PCRAM possible. The *R-I* plot serves as an important design tool for the WRITE process. For a given programming duration (500 ns), the amplitude of the programming pulse can be determined from the corner of abrupt resistance change (~ 0.2 V for SET pulse and ~ 1.8 V for RESET pulse). Note that the resistance change is smoother during the transition from the amorphous state to the crystalline state.

III. Macromodel

Architecture and Operation

The model architecture (Fig. 5) is intrinsically a feedback system, which is composed of three building blocks: the decision circuit, the phase change circuit, and the logic circuit. The input and output of the system are the programming current pulses and the PCRAM output state. Initially, the PCRAM can be under any state, which is recorded by the decision circuit. The phase change circuit assumes this state at the start and computes the PCRAM temperature characteristic and its crystallization fraction. Subsequently, the logic circuit delivers the phase change information to the decision circuit. This model architecture can also simulate the ML operation of the PCRAM with more complex logic circuit and some minor addition of the other two building blocks [1]. Actually, the binary level operation of the PCRAM can be viewed as a special case of the ML operation. Since they have a similar operation scheme, the discussion of implementation details mainly deals with the binary-level operated PCRAM.

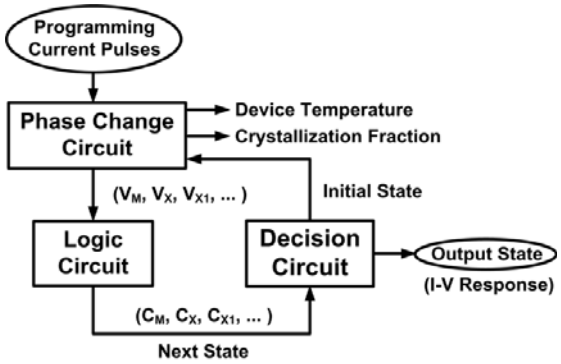


Fig. 5. Architecture of the macromodel.

Implementation

This work is simulated with the SPICE simulator Eldo, which provides a good library of behavior models. Among them, comparators, switches, integrators, logic gates, and a peak detector are utilized to gain model efficiency. Governing equations of the PCRAM operation [1] are not treated here for the brevity of the paper.

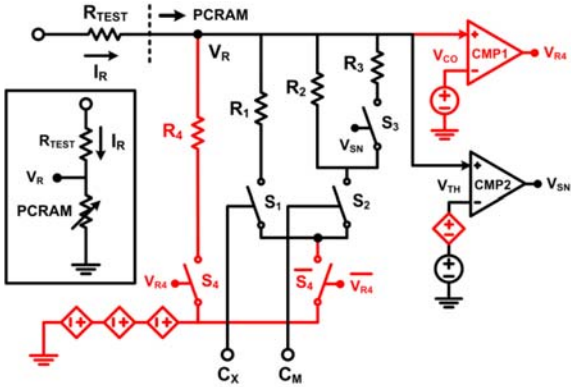


Fig. 6. Implementation of the decision circuit.

Decision Circuit: The decision circuit (Fig. 6) accounts for the resistance switching of the PCRAM. It is basically a combination of resistors and switches, which are realized by voltage-controlled resistors. Enlightened by Fig. 3, there should be disparate resistors dealing with the four regions of the *I-V* plot. The resistors R_1, R_2, R_3 and R_4 correspond to Region 1, 2, 3, and 4, respectively. The resistor R_{TEST} is the testing resistor in series of the PCRAM for the detection of the snapback phenomenon. The inset shows the testing setup. The enhancement of the decision circuit is marked in red. If the voltage across the PCRAM (V_R) is lower than the voltage that makes both states converge (V_{CO}), the switch S_4 will be turned off and $\overline{S_4}$ turned on. It depends on the logic circuit outputs (C_X and C_M) to have the resistor R_1 or the resistor R_2 connected (Region 1 or Region 2). Under the condition of Region 2, if V_R is larger than the switching threshold voltage (V_{TH}), the switch S_3 will be turned on to connect R_2 and R_3 in parallel, producing a lower resistance (Region 3). On the other hand, if V_R is larger than V_{CO}, the switch S_4 will be turned on and $\overline{S_4}$ turned off, leaving only the resistor R_4 connected (Region 4). In the enhanced decision circuit, four auxiliary voltage controlled voltage source (VCVS) are added for the purpose of *I-V* continuity compensation.

Phase Change Circuit: The phase change circuit (Fig. 7) calculates the PCRAM temperature and the crystallization fraction. The

VCVS G_J monitors the programming power into the PCRAM, and the VCVS G_D monitors the heat dissipation out of the PCRAM, which is subtracted from G_J for the net power. Integrator INT1 calculates the device temperature T_R, which is compared with T_M and T_{GT} for the outputs V_M and V_{XP}, respectively. The falling edge correction circuit (FECC) together with the XOR and AND gates before the integrator INT2 (blue part) works to correct the falling edge problem, which is illustrated in Fig. 8. Prior to the enhancement, the input of INT2 (C_{EN}) is directly connected to V_{XP} for crystallization time accumulation. The falling edge of the temperature characteristic (Segment S3) indicates the cooling down after the PCRAM is melted, so the PCRAM should remain in the amorphous state. However, because the comparators CMP3 and CMP4 cannot distinguish Segment S3 from Segment S1 (both with $V_M = 0$ and $V_{XP} = 1$), the PCRAM will be misinterpreted as in the crystalline state. As for the other part of the falling edge (Segment S4), due to $V_M = V_X = 0$, the PCRAM will keep its previous state by the logic circuit operation.

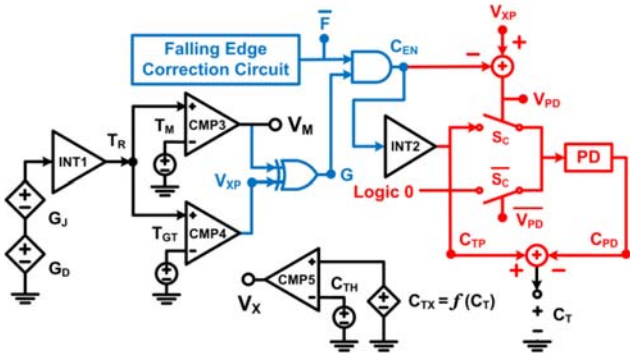


Fig. 7. Implementation of the phase change circuit.

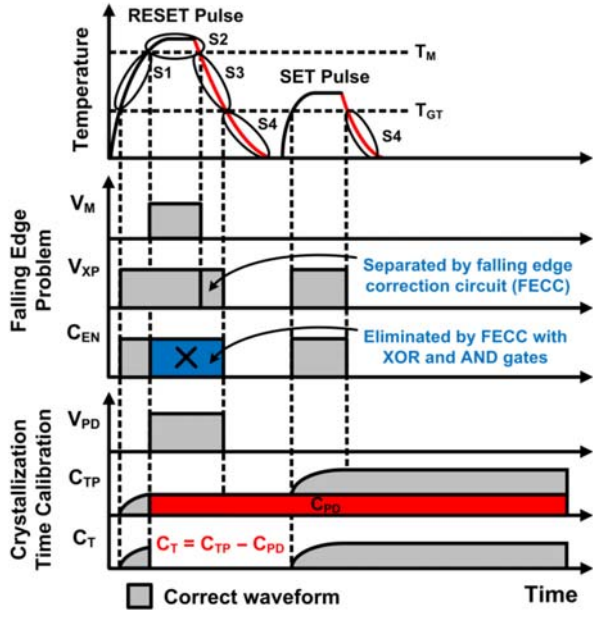
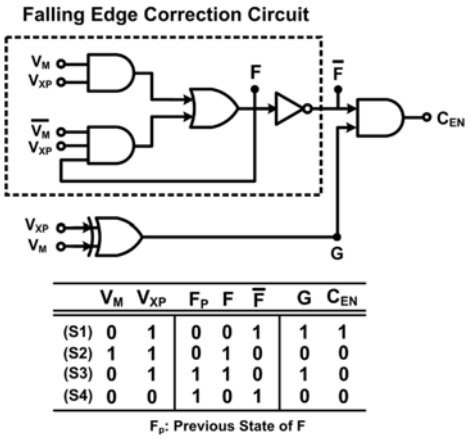


Fig. 8. Illustration of the falling edge problem and the crystallization time calibration.

To rectify the falling edge problem, the FECC first separate Segment S3 from Segment S1 by feeding its previous output (F) back as one of the inputs (Fig. 9). The truth table of the FECC with the XOR and AND gates is also demonstrated in Fig. 9. Segment S3 ($V_M = 0$, $V_{XP} = 1$, $F_P = 1$ due to the previous S2 state) produces the output $\bar{F} = 0$ to the following AND gate, making $C_{EN} = 0$. This is different from the result of Segment S1 ($C_{EN} = 1$). For Segment S2 ($V_M = V_{XP} = 1$) or Segment S4 ($V_M = V_{XP} = 0$), the effect $\bar{F}$ will be nullified by the following AND gate because G = 0. As a result, the unwanted part of the C_{EN} waveform (blue area) is eliminated. The peak detector (PD) together with two adders and the switch pair following INT2 (red part) works to calibrate the accumulated crystallization time (C_T). Because INT2 integrates accumulatively since t = 0 without the notice of PCRAM state change, the crystallization time after two distinct pulses is wrong (Fig. 8). To solve this problem, the crystallization time must be reset to zero after the PCRAM reaches the amorphous state. The PD together with the switch pair records the excessive crystallization time (C_{PD}), which is deducted from the wrong waveform (C_{TP}) to obtain the calibrated C_T. Finally, the VCVS C_{TX} produces the crystallization fraction, which is compared with C_{TH} (100% in binary level operation) to have V_X.

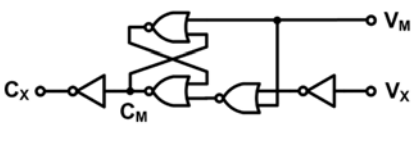


	V_M	V_{XP}	F_P	F	$\bar{F}$	G	C_{EN}
(S1)	0	1	0	0	1	1	1
(S2)	1	1	0	1	0	0	0
(S3)	0	1	1	1	0	1	0
(S4)	0	0	1	0	1	0	0

F_p: Previous State of F

Fig. 9. Implementation of the circuit to solve the falling edge problem and its truth table.

Logic Circuit: The logic circuit communicates between the phase change circuit and the decision circuit. The implementation of the logic circuit (5 logic gates) and its truth table are shown in Fig. 10. The gate count should be minimized for a compact macromodel. As mentioned previously, for ML operation of the PCRAM, a more complicated logic circuit is needed. As a demonstration for 2-bit operation of the PCRAM, the implementation of the logic circuit (26 logic gates) and its truth table are disclosed in Fig. 11.



Logic Circuit for 1-bit PCM Model

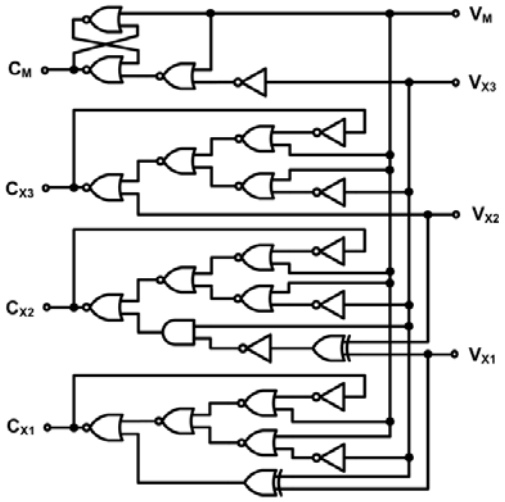
V_M	V_X	C_M	C_X
0	0	Q_p	$\bar{Q}_p$
1	0	1	0
1	1	1	0
0	1	0	1

Q_p: Previous State

Fig. 10. Implementation of the logic circuit and its truth table.

IV. Model Verification

The model verification of the *I-V* plot (Fig. 12) and the *R-I* plot (Fig. 13) shows good correlation between the measurement (Fig. 3 and Fig. 4) and the macromodel. Snapback phenomenon is clearly modeled in Fig. 12. The behavior of the smooth transition from the amorphous state to the crystalline state should be studied further to better fit this region of the *R-I* curve.



Logic Circuit for 2-bit PCM Model

V_{X3}	V_{X2}	V_{X1}	V_M	C_{X3}	C_{X2}	C_{X1}	C_M
0	0	0	0	Q_p	Q_p	Q_p	Q_p
1	0	0	0	1	0	0	0
1	1	0	0	0	1	0	0
1	1	1	0	0	0	1	0
X	X	X	1	0	0	0	1

X: Don't-Care Q_p: Previous State

Fig. 11. Implementation of the logic circuit for ML (2-bit) PCRAM operation and its truth table.

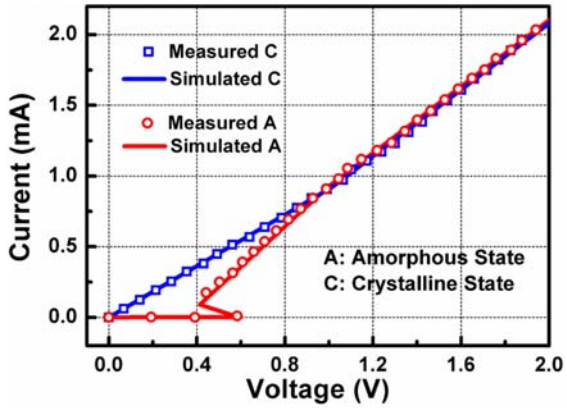


Fig. 12. Model verification of the *I-V* plot.

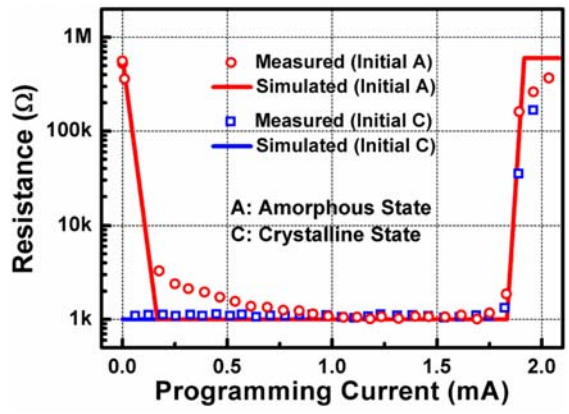


Fig. 13. Model verification of the *R-I* plot.

The device temperature (T_R) and the crystallization fraction (C_{TX}) can be extracted from the macromodel (Fig. 14). For modeling of ML operation of the PCRAM, the relationship between the SET pulse and C_{TX} should be clearly characterized.

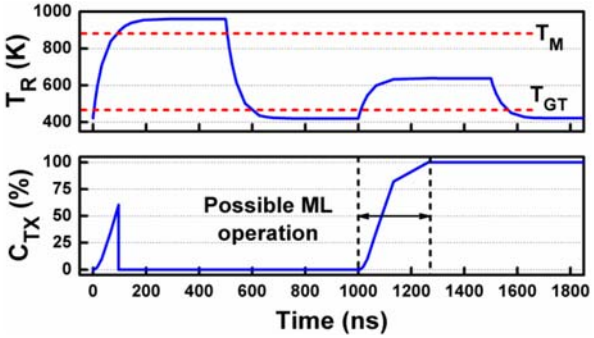


Fig. 14. Crystallization fraction indicated by the macromodel.

V. Conclusion

The improved SPICE macromodel of the PCRAM solves critical problems in the phase change circuit to produce accurate *I-V* curve with clearly modeled snapback behavior. The *R-I* curve is also in good agreement with the measured data. Besides, the crystallization fraction can be extracted from the macromodel, which is useful for potential ML operation of the PCRAM. Additionally, the underlying idea can be applied to RRAM modeling [6] because of their similar operation scheme.

Acknowledgment

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References

[1] X. Q. Wei, L. P. Shi, R. Walia, T. C. Chong, R. Zhao, X. S. Miao, and B. S. Quek, "HSPICE macromodel of PCRAM for binary and multilevel storage," *IEEE Tran. Electron Device*, vol. 53, no. 1, pp. 56-62, Jan. 2006.

[2] Y.-B. Liao, Y.-K. Chen, M.-H. Chiang, "Phase change memory modeling using Verilog-A," in *Proc. IEEE International Behavioral Modeling and Simulation Conference*, pp. 159-164, Sep. 2007.

[3] A. Redaelli, A. L. Lacaita, A. Benvenuti, and A. Pirovano, "Comprehensive numerical model for phase-change memory simulations," in *Proc. International Conference on Simulation of Semiconductor Processes and Devices*, pp. 279-282, Sep. 2005.

[4] R. A. Cobley, and C. D. Wright, "Parameterized SPICE model for a phase-change RAM device," *IEEE Tran. Electron Device*, vol. 53, no. 1, pp. 112-118, Jan. 2006.

[5] D. Ventrice, P. Fantini, A. Redaelli, A. Pirovano, A. Benvenuti, and F. Pellizzer, "A phase change memory compact model for multilevel applications," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 973-975, Nov. 2007.

[6] J.-G. Lee, D. H. Kim, J. G. Lee, D. M. Kim, and K.-S. Min "A compact HSPICE macromodel of resistive RAM," *IEICE Electronics Express*, vol. 4, no. 19, pp. 600-605, Oct. 2007.